DIGITAL

Ph.D Preliminary Exam questions

Fall 2012

Name: _____ Date: October 26, 2012

Boolean algebra and logic minimization:

1. The input/output function is specified as $f(x_1, x_2, x_3, x_4) = \sum m(2,4,5,6,10) + D(12, 13, 14, 15)$ where D is the set of don't-cares. Use K-map to simplify the function to the simplest SOP implementation and POS implementation. How many logic gates are needed for the two implementations respectively?

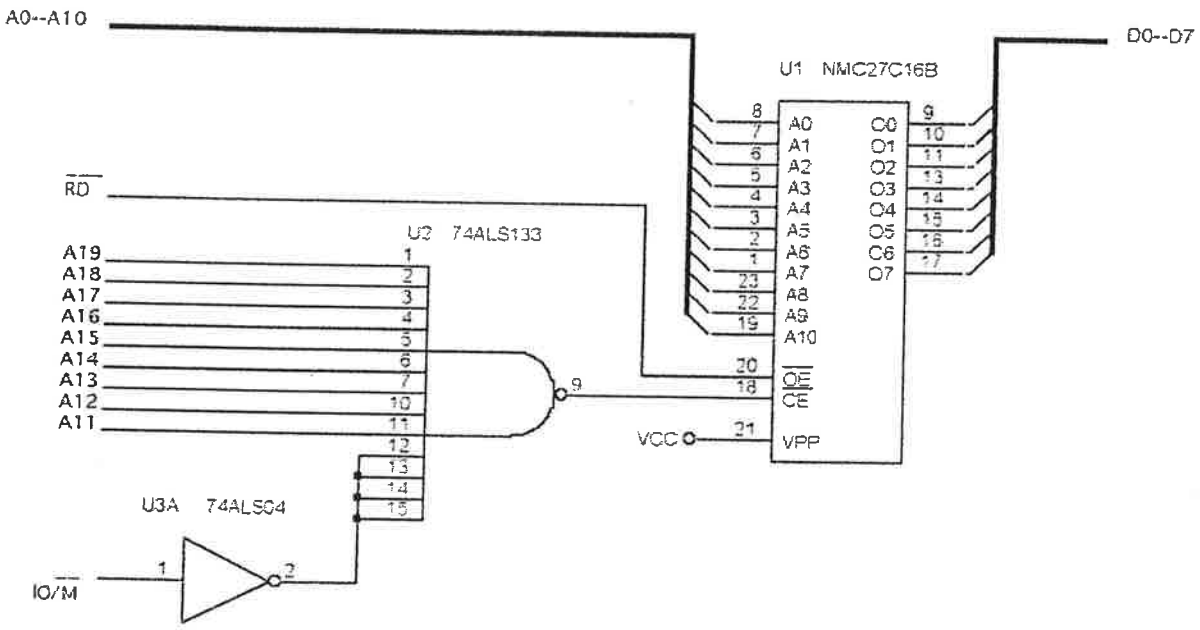
Computer instructions and addressing modes

2. Explain the following 68000 assembly program using flowchart. A8, B8, and R8 are three 8-bit variables. What is the purpose for this program? Pick up two different addressing modes from the program, what type of addressing modes are they? (Assembly language instructions are provided as attached.)

```
            ldaa    A8
            adda    B8
            bvc     ok3
err3        bpl     under3
            ldaa    #127
            bra     ok3
under3      ldaa    #-128
ok3         staa    R8
```

Design of a CPU input-output communication memory management

3. Below figure is a simple NAND gate decoder that selects a 2716 EPROM for memory location.
   a. What is the address range?
   b. Modify the NAND gate decoder to select the memory for address range DF800H – DFFFFH.
   c. Modify the NAND gate decoder to select the memory for address range 40000H – 407FFH.
   d.



5. Design a finite-state controller for an obstacle robot.

Description: The robot is to maneuver by turning whenever it comes in contact with an obstacle. On the nose of the robot is a sensor whose output X=1 whenever it is in contact with an obstacle; X=0 otherwise. The robot has two control lines: Z_1=1, which turns the robot to the left, and Z_2=1 which turns the robot to the right. When it encounters an obstacle, the robot should turn right until no obstacle is detected. The next time an obstacle is detected, the robot should turn left until the obstacle is cleared, and so on.

The robot controller requires 4 states as follows:

State A= no obstacle detected, last turn was left
State B= obstacle detected, turning right
State C= no obstacle detected, last turn was right
State D=obstacle detected, turning left

Draw the circuit for the controller using D flip-flops.

Ph.D. Preliminary Examination
in
Digital Systems

Spring 2012

Write legibly.
No points will be given for answers that show no work.

Do not use cell phone and calculator during the examination.

Note: Each problem is worth 20 points.

Name: _____ **Date: March 30, 2012**

1. Assume that a crystal clock oscillator on a hardware board operates at 25 MHz. We would like to operate a state machine on the board at a much slower frequency. What would be the minimum number of bits or FFs for a binary counter that could be used to slow this clock oscillator frequency down to slightly less than 1 Hz . What signal assignment must be made to signal *slow_clk* to operate the state machine on the board at the slower frequency?

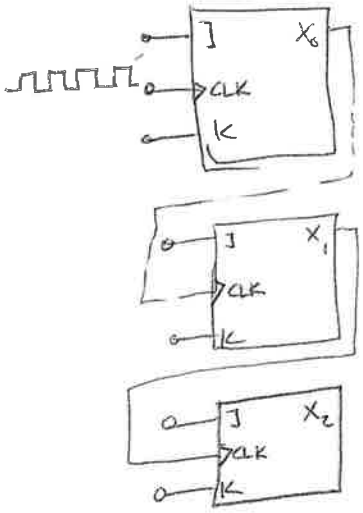
Frequency Division. $\Rightarrow \frac{25\text{MHz}}{1\text{Hz}} = 25,000,000$

Division factor $> 25,000,000$

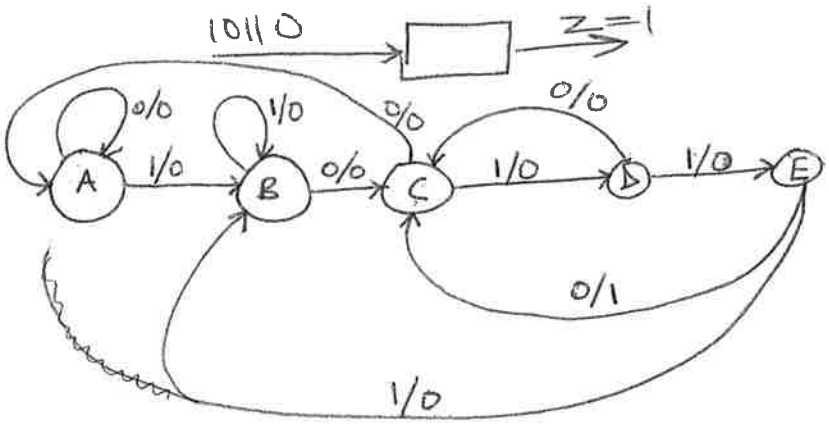
$2^{24} < 25,000,000 < 2^{25}$

Hence minimum number of FFs $= 25$

The clock is applied to the CLK input of the 1st FF while the output of the FFs are used to clock subsequent FFs



2. Design a circuit to detect the sequence 10110. Include the state diagram and circuit.



Mealy model
output depends on input + present state

State table

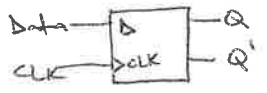
Present State	Next State X=0	Next State X=1	Output Z X=0	Output Z X=1
A	A	B	0	0
B	C	B	0	0
C	A	D	0	0
D	C	E	0	0
E	C	B	1	0

Let A = 000
B = 001
C = 010
D = 011
E = 100

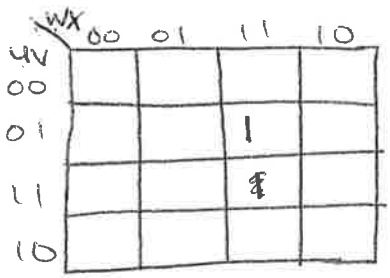
⇒

Present State u v w	Next State X=0	Next State X=1	Output Z X=0	Output Z X=1
000	000	001	0	0
001	010	001	0	0
010	000	011	0	0
011	011	100	0	0
100	011	001	1	0

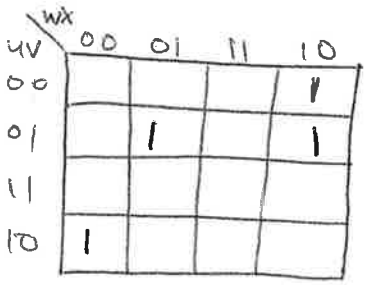
Using D Flip-Flop



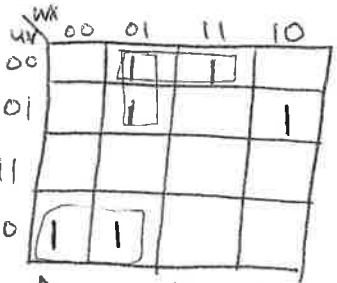
D	Q(t+1)
0	0
1	1



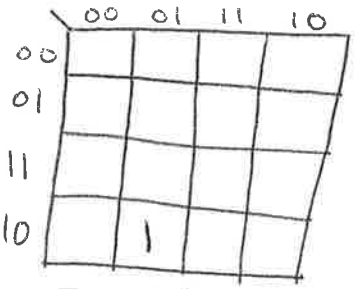
$D_u = \bar{u}vwx$



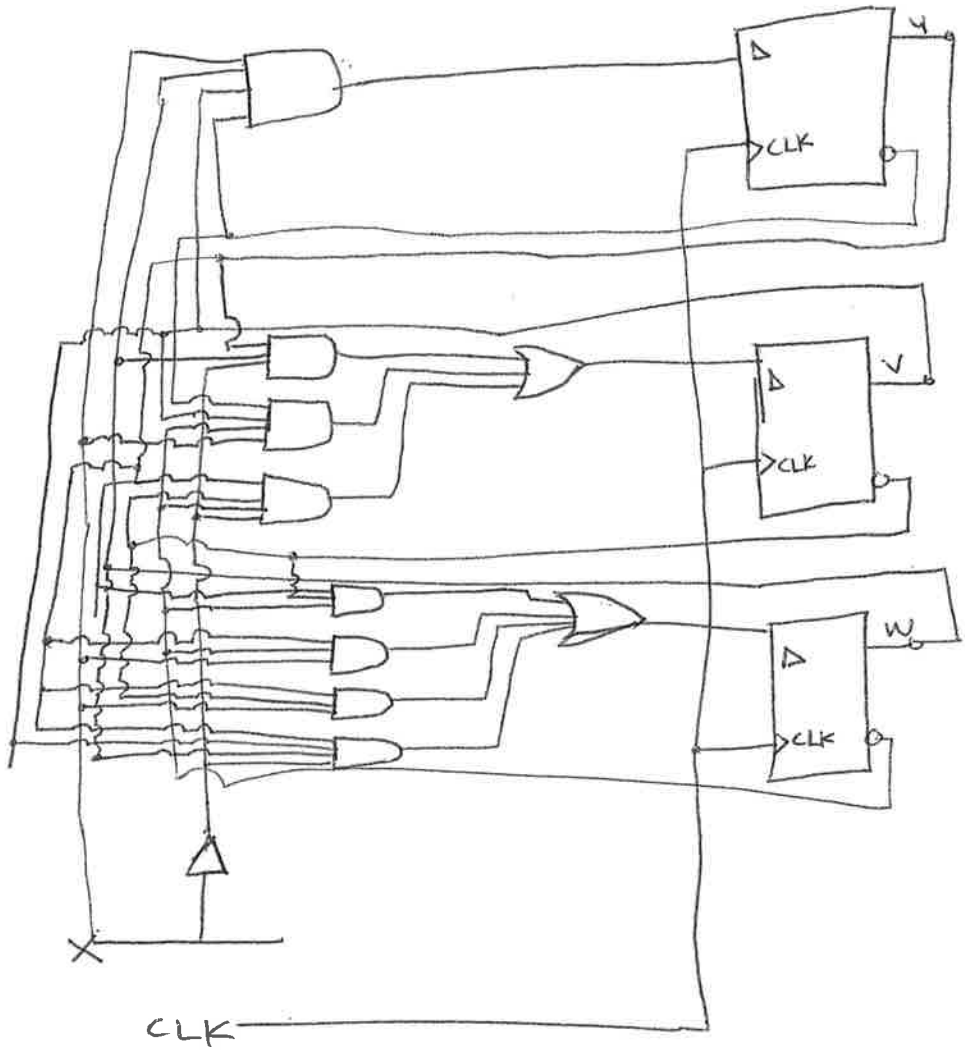
$D_v = uw\bar{x} + \bar{u}v\bar{w}x + uv\bar{w}\bar{x}$



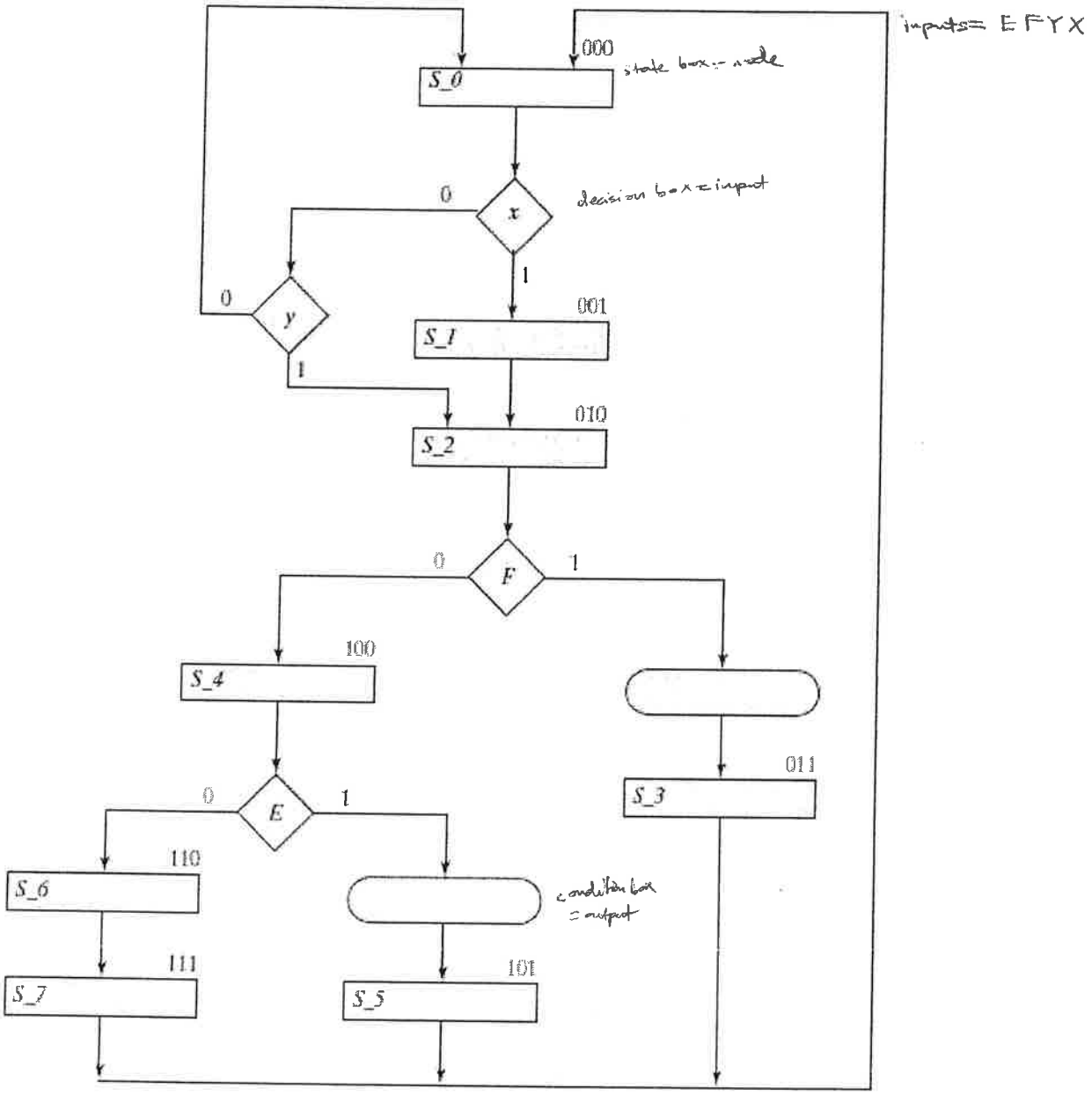
$D_w = u\bar{v}\bar{w} + \bar{u}\bar{w}x + \bar{u}\bar{v}x + \bar{u}vw\bar{x}$

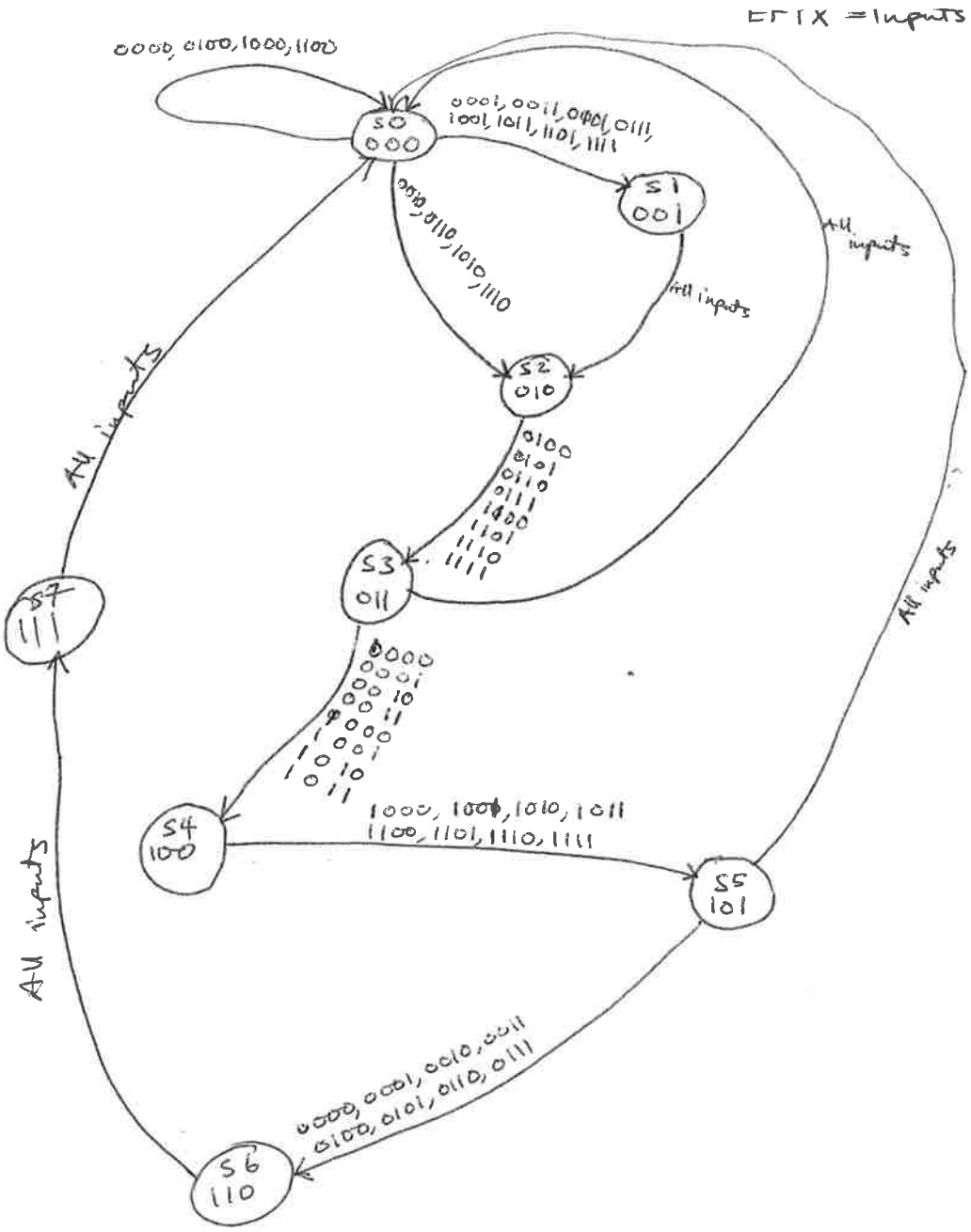


$Z = u\bar{v}\bar{w}x$


Y
CLK
V
CLK
W
CLK
X
CLK

3. An ASMD chart for a finite state machine is shown. The register operations are not specified, because we are interested in designing the control logic.
    a. Draw the equivalent state diagram
    b. Design the control unit. Draw the circuit
    c. List the state table for the control unit.




FFIX = inputs
0000, 0100, 1000, 1100
S0
000
0001, 0011, 0101, 0111,
1001, 1011, 1101, 1111
S1
001
0010, 0110, 1010, 1110
All inputs
All inputs
S2
010
0100
0101
0110
0111
1000
1001
1010
1011
S3
011
All inputs
All inputs
S7
111
0000
0001
0010
0011
0100
0101
0110
0111
S4
100
1000, 1001, 1010, 1011
1100, 1101, 1110, 1111
S5
101
All inputs
0000, 0001, 0010, 0011
0100, 0101, 0110, 0111
S6
110

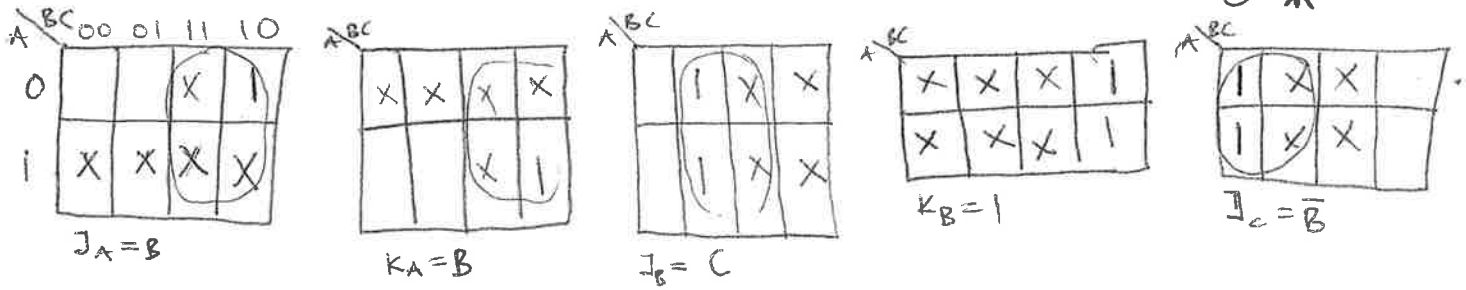
4. Design a 4-bit aritmetic circuit with two selection variables S_1 and S_0 that generates the following arithmetic operations:

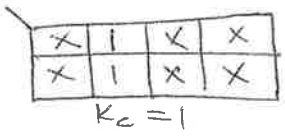
S_1 S_0	$C_{in} = 0$	$C_{in} = 1$
0 0	$F = A + B$ (add)	$F = A + B + 1$
0 1	$F = A$ (transfer)	$F = A + 1$ (increment)
1 0	$F = \overline{B}$ (complement)	$F = \overline{B} + 1$ (negate)
1 1	$F = A + \overline{B}$	$F = A + \overline{B} + 1$ (subtract)

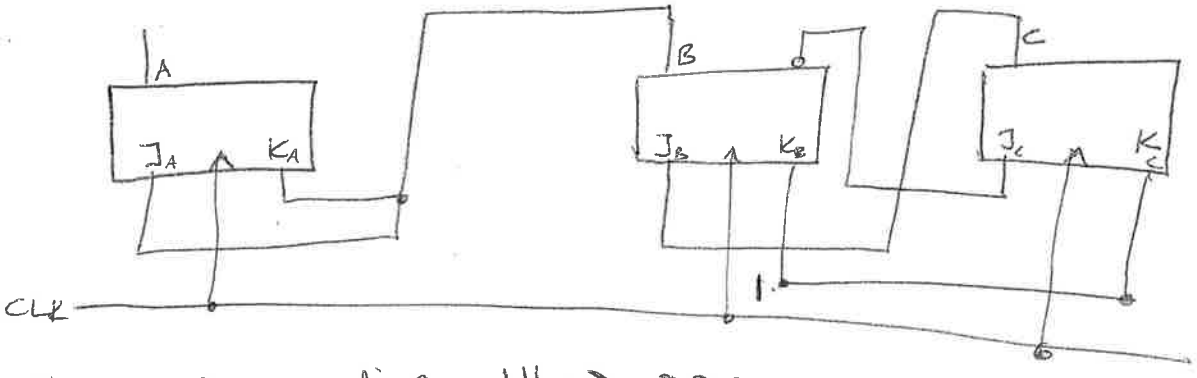
Draw the logic diagram for a single bit stage.

5. Use JK-type flip-flops to design a 3-bit self-correcting counter with the repeated binary sequence: 0, 1, 2, 4, 5, 6. Note that there are two unused states, 3 and 7, and the counter is self-correcting (if the circuit ever goes to one of the unused states, the next count pulse transfers it to one of the valid states and continues to count correctly).

Present state A B C	Next state A B C	FF Inputs J_A	K_A	J_B	K_B	J_C	K_C
0 0 0	0 0 1	0	X	0	X	1	X
0 0 1	0 1 0	0	X	1	X	X	1
0 1 0	1 0 0	1	X	X	1	0	X
1 0 0	1 0 1	X	0	0	X	1	X
1 0 1	1 1 0	X	0	1	X	X	1
1 1 0	0 0 0	X	1	X	1	0	X







H is self correcting 111 → 000

011 → 100

Digital System Design

Fall 2011 Preliminary Exam Questions

Name: _____ **Date:** _____

Each problem is worth 10 points.

Problem	Max Points	Student Points
Problem 1	10	
Problem 2	10	
Problem 3	10	
Problem 4	10	
Problem 5	10	
Problem 6	10	
Total	60	

$$\text{Score} = \frac{\qquad\qquad}{60} * 100\% = \_\_\_\_\_$$

1. Design a combinational circuit that compares two four-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal to 0 otherwise.

2. Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number.

4. A traffic metering system for controlling the release of traffic from an entrance ramp onto a superhighway has the following specifications for a part of its controller. There are three parallel metering lanes, each with its own stop (red) - go (green) light. One of these lanes, the car pool lane, is given priority for a green light over the other two lanes. Otherwise, a "round robin" scheme in which the green lights alternate is used for the other two (left and right) lanes. The part of the controller that determines which light is to be green (rather than red) is to be designed. The specifications for the controller follow:

Inputs

PS Car pool lane sensor (car present – 1: car absent-0)
LS Left lane sensor (car present – 1: car absent-0)
RS Right lane sensor (car present – 1: car absent-0)
RR Round robin signal (select left – 1; select right -0)

Outputs

PL Car pool lane light (green-1; red – 0)
LL Left lane light (green-1; red – 0)
RL Right lane light (green-1; red – 0)

Operation

1. If there is a car in the car pool lane, PL is 1.
2. If there are no cars in the car pool lane and the right lane, and there is a car in the left lane, LL is 1.
3. If there are no cars in the car pool lane and in the left lane, and there is a car in the right lane, RL is 1.
4. If there is no car in the car pool lane, there are cars in both the left and right lanes and RR is 1, then LL=1.
5. If there is no car in the car pool lane, there are cars in both the left and right lanes, and RR is 0, then RL =1.
6. If any PL, LL or RL is not specified to be 1 above, then it has value 0

   a. Find the minimum multiple-level gate implementation with minimum gate input cost using AND gates, OR gates and inverters.

6. Design a digital system with three 16-bit registers AR, BR, and CR and 16-bit data input IN to perform the following operations, assuming a 2s complement representation and ignoring overflow:
    a. Transfer two 16-bit signed numbers to AR and BR on successive clock cycles after a go signal G becomes 1.
    b. If the number in AR is positive but nonzero, multiply the contents of BR by two and transfer the result to a register CR.
    c. If the number AR is negative, multiply the contents of AR by two and transfer the result to register CR.