

Digital Design Preliminary Exam (Fall 2010)

Name or Student ID:

Date: 10/29/2010

| Question No. | Percentage % | Grade |
|--------------|--------------|-------|
| 1 | 15 | |
| 2 | 15 | |
| 3 | 15 | |
| 4 | 10 | |
| 5 | 15 | |
| 6 | 10 | |
| 7 | 20 | |

Problem 1: Numbers.

- a. Inside a computer, negative numbers are represented by 2's complement. And subtraction can also be completed as add a negative number in 2's complement form. Use 8-bit binary to illustrate the signed operation of $-96 - 64$ and explain why or why not an overflow occur?

$$\begin{array}{r}
 64 = 01000000 \\
 96 = 01100000 \\
 \hline
 \begin{array}{r}
 \text{2's complement} \\
 -96 = 11000000 \\
 -64 = 10100000 \\
 \hline
 101100000
 \end{array}
 \end{array}$$

- b. IEEE 754 standard in using 32 bits to code a floating point value has 8 bits for exponent and 23 bits for fraction. The bias is 127_{10} . Based on this standard, below binary represents which decimal floating point value? (Show the procedure.)

01000001100101000000000000000000

Sign bit → 0 | 10000001 | 100101000000000000000000

E

$$N = (-1)^S (1+F) (2^{E-127})$$

~~0100~~ 10000001 = $2^7 + 2^1 + 2^0 = 131$

$$= (-1)^0 (1 + 0.00101) (2^{131-127})$$

$$= (1.00101) 2^4 = +$$

$$\approx \frac{3}{16} \cdot 2^4 = 3.0$$

$$N = (-1)^S (1+F) 2^{E-127}$$

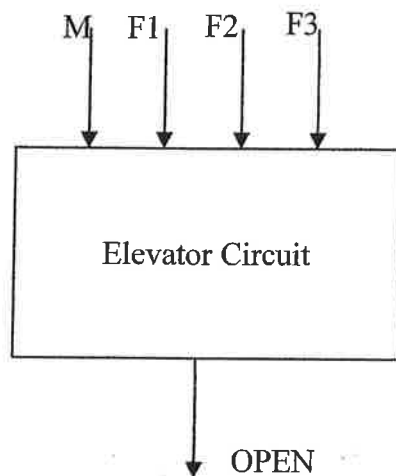
$$N = (-1)^S (1+F) (2^{E-127})$$

$$\begin{array}{cccc}
 -1 & -2 & -3 & \dots \\
 2^{-1} & 0 & 0 & 2^{-p} \\
 \frac{1}{2} + \frac{1}{4} = \left(\frac{3+1}{4}\right) 2 = \frac{3}{2}
 \end{array}$$

Problem 2: Boolean algebra and minimization methods.

Design a logic circuit that controls the elevator door in a three-story building. The circuit has four inputs. M is a logic signal that indicates when the elevator is moving (M=1) or stopped (M=0). F1, F2, and F3 are floor indicator signals that are normally LOW, and they go HIGH only when the elevator is positioned at the level of that particular floor. For example, when the elevator is lined up level with the second floor, F2=1 and F1=F3=0. The circuit output is the OPEN signal, which is normally LOW and will go HIGH when the elevator door is to be opened. Find the simplified design and draw the diagram of the elevator circuit.

Note: Because the elevator cannot be lined up with more than one floor at a time, the cases when more than one floor inputs are high can be treated as don't care condition. When the elevator reaches at one floor and stops, the door opens. Utilize K map to minimize the output expression.)



| M | F ₁ | F ₂ | F ₃ | OUTPUT |
|---|----------------|----------------|----------------|--------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | X |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | X |
| 0 | 1 | 1 | 0 | X |
| 0 | 1 | 1 | 1 | X |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

| M F ₁ | F ₂ F ₃ | | | |
|------------------|-------------------------------|----|----|----|
| | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | X | 1 |
| 01 | 1 | X | X | X |
| 11 | | X | X | X |
| 10 | | | X | |

$$\text{OUTPUT} = \bar{M}F_1 + \bar{M}F_3 + \bar{M}F_2$$

$$\text{OUTPUT} = \bar{M}(F_1 + F_2 + F_3)$$

Problem 3: Combinational design with multiplexer.

For the function $f(A, B, C) = \sum m(0, 4, 5, 6)$, use Shannon's expansion to derive an implementation using a 2-to-1 multiplexer and any other necessary gates.

$$f(A, B, C) = M_0 + M_4 + M_5 + M_6$$

$$= A'B'C' + AB'C' + AB'C + ABC'$$

Shannon

$$f(A, B, C) = \bar{A} \cdot f(0, B, C) + A \cdot f(1, B, C)$$

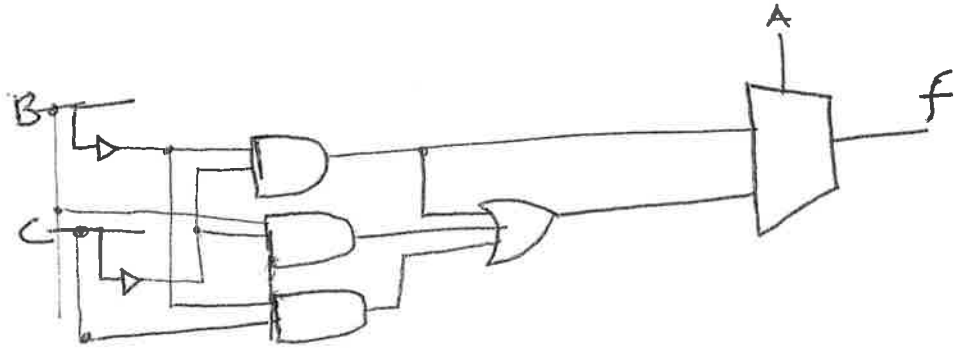
$$\bar{A} \cdot (B'C') + A \cdot (B'C' + B'C + BC')$$

| A | f |
|---|--------------------|
| 0 | $B'C'$ |
| 1 | $B'C' + B'C + BC'$ |

Truth Table

| A | B | C | f |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

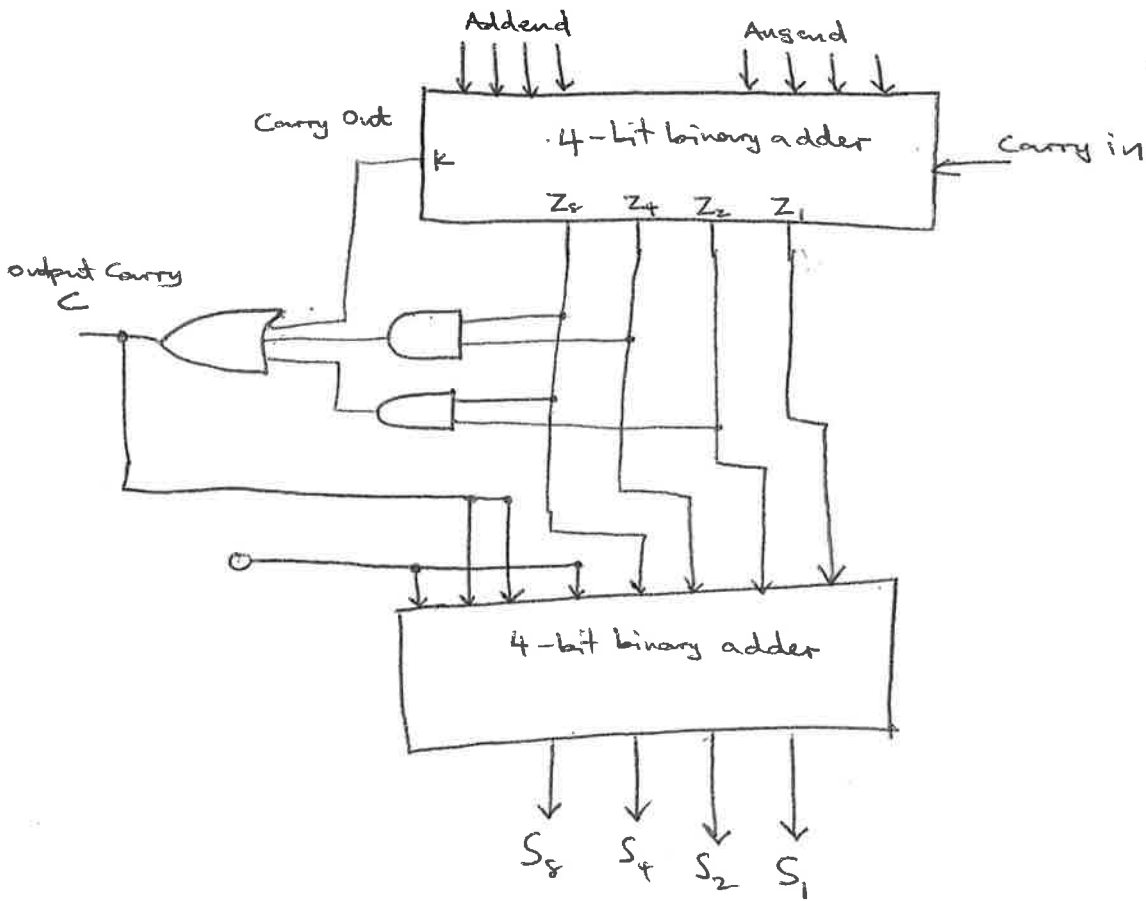
| A | f |
|---|--------------------|
| 0 | $B'C'$ |
| 1 | $B'C' + B'C + BC'$ |



Problem 4: Digital design and code.

Use two 4-bit binary adders and other basic logic gates to build a BCD adder. This BCD adder should also have carry in and carry out bits.

Binary Sum B C D Sum
 $K \ Z_8 \ Z_4 \ Z_2 \ Z_1$ $C \ Z_8 \ Z_4 \ Z_2 \ Z_1$
 C = condition for correction
 $C = K + Z_8 Z_4 + Z_8 Z_2$

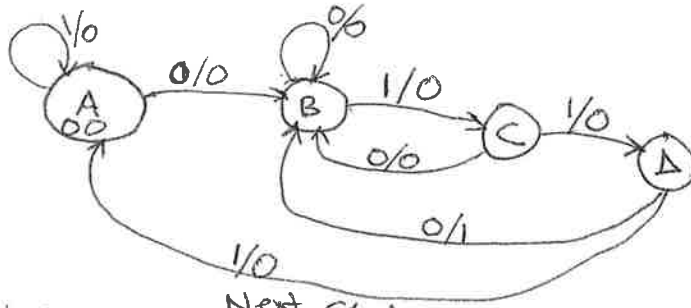


Problem 6: Design a digital combination lock for the specifications below.

Specification:

- 2 inputs ("0" and "1" buttons)
- One output ("OPEN" signal)
- UNLOCK is 1 if and only if: Last 4 button pressed were the "combination": 0110

A = 00
 B = 01
 C = 10
 D = 11

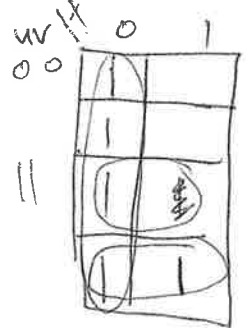
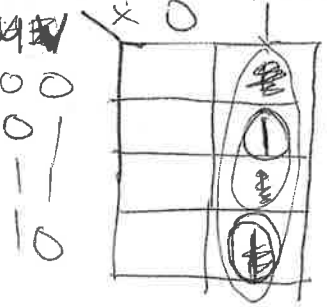


| State | Present state | Next state |
|-------|---------------|------------|
| A | 00 | 00 |
| B | 01 | 01 |
| C | 10 | 10 |
| D | 11 | 11 |

| Next state | x | |
|------------|-----|-----|
| | x=0 | x=1 |
| 00 | 01 | 00 |
| 01 | 01 | 10 |
| 10 | 01 | 11 |
| 11 | 01 | 00 |

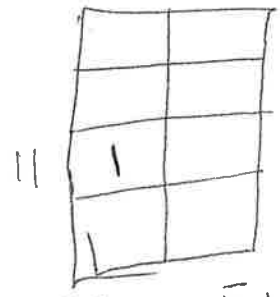
| Output | x | |
|--------|-----|-----|
| | x=0 | x=1 |
| 0 | 0 | 0 |
| 0 | 0 | 0 |
| 0 | 0 | 0 |
| 1 | 0 | 0 |

Using D-Flip Flop

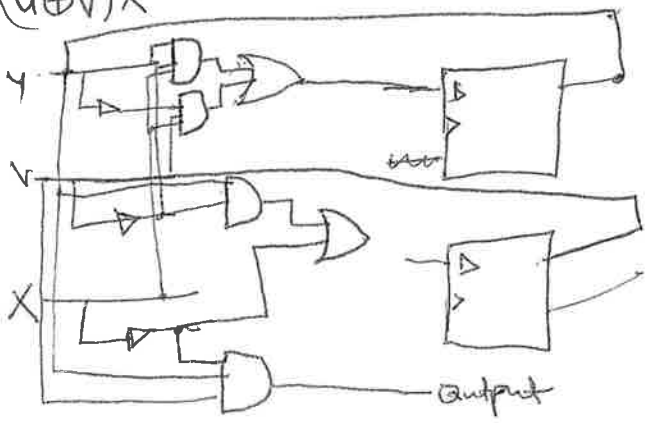


$$D_u = \bar{u}\bar{v}x + \bar{u}vx + u\bar{v}x + uvx = (u \oplus v)x$$

$$D_v = \bar{x} + uv'$$



$$\text{Output} = \bar{x}uv$$



Problem 7:

You are an engineer working for NASA. They want you to design a FSM that will test their newest rover Fido on the PVAMU campus. NASA wirelessly transmits the travel plans to Fido, and then Fido moves according to that information.

To design your FSM, you first select the following locations around the PVAMU campus and assign each location with a state in 3-bit binary representation:

S. R. Collins Engr Bldg [000], Electrical Engr Bldg [001], C. L. Wilson/Gilchrist Engr Bldg [010], Chemical Engr Bldg [011], University College [100], University Village Phase 1 & 2 [101], Home Economics Building [110], and the Delco Building [111].

To simplify your test, you inform NASA to send Fido's FSM a binary sequence for travel plans

(e.g. '1-0-0-0-1' to cause Fido to move five times). In other words, Fido receives either '0' or '1' for each move and travels to the next destination as specified below. Fido starts off at the S. R. Collins Engr Bldg for each test run, and your FSM should output Fido's current location.

| | | |
|--|---|--|
| S. R. Collins Engr Bldg [000] | If 0, stay at S. R. Collins Engr Bldg | If 1, go to Electrical Engr Bldg |
| Electrical Engr Bldg [001] | If 0 go to C. L. Wilson/Gilchrist Engr Bldg | If 1, go to University College |
| C. L. Wilson/Gilchrist Engr Bldg [010] | If 0, go to Chemical Engr Bldg | If 1, go to University College |
| Chemical Engr Bldg [011] | If 0, stay at Chemical Engr Bldg | If 1, go to S. R. Collins Engr Bldg |
| University College [100] | If 0, go to Delco Building | If 1, go to University Village Phase 1 & 2 |
| University Village Phase 1 & 2 [101] | If 0, go to Chemical Engr Bldg | If 1, go to Home Economics Bldg |
| Home Economics Bldg [110] | If 0, go to Delco Building | If 1, stay at Home Economics Bldg |
| Delco Building [111]. | If 0, go to Electrical Engr Bldg | If 1, go to University Village Phase 1 & 2 |

- Draw the circuit for the FSM using D flip-flops. Show all work for full credit
- If Fido is forever given a sequence of ones (i.e. 11111...), where will it eventually end up?

Final location: Home Economics (110)

- If Fido is forever given a sequence of 01s (i.e. 010101...), which location(s) will

it never visit?

Location(s) never visited: 110

