

## **ASSIGNMENTS FOR OUTCOME 6**

**An ability to develop and conduct appropriate experimentation, analyze and interpret data and use engineering judgement to draw conclusions.**

# ELECTRICAL & COMPUTER ENGINEERING OUTCOMES

## SPECIFIC ASSIGNMENT COVER SHEET

ELEG 3063 Logic Circuits

FALL 2020

Instructor: H. St. Julian

### Title of Assignment

Design a circuit that functions as an 8 to 3 encoder when an enable bit is set to 1 and as an 8x1 multiplexer when the enable bit is set to zero.

### Outcome Measured Using this Assignment

Outcome 6

An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions

**Check the experimentation problem characteristics related to this assignment**

|                                                                                                                               |                                                                                                                    |
|-------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|
| <b>Ability to develop experiment</b><br>Requires students to                                                                  |                                                                                                                    |
| X                                                                                                                             | Identify the appropriate parameters or variables and relationships (independent, dependent and control variables). |
| X                                                                                                                             | Identify and select appropriate equipment or components for measuring the parameters                               |
| X                                                                                                                             | Provide steps for setting up and conducting the experiment and                                                     |
|                                                                                                                               | Identify data collection method to support experiments (if needed)                                                 |
| <b>Ability to conduct experiments</b><br>Requires students to                                                                 |                                                                                                                    |
| X                                                                                                                             | Conduct experiment while maintaining all safety precautions                                                        |
| X                                                                                                                             | Demonstrate knowledge of how to use the equipment safely                                                           |
|                                                                                                                               | Collect and record data using appropriate units of measurement and significant figures                             |
| <b>Ability to analyze and interpret experimental data</b><br>Requires students to                                             |                                                                                                                    |
| X                                                                                                                             | Present the data (raw /derived) in tabular or graphical form to meet the objectives and to aid in interpretation   |
|                                                                                                                               | Use appropriate statistical analysis methods to analyze and interpret data                                         |
|                                                                                                                               | discuss the raw and derived data/graphs and assess the validity of the results                                     |
| <b>Demonstrate the use of engineering judgement in the development and analysis of the experiment</b><br>Requires students to |                                                                                                                    |
| X                                                                                                                             | Draw appropriate conclusions and recommendations using engineering judgement.                                      |

### Brief justification of the suitability of assignment for the outcome

After the students complete the paper design, they implement and test the circuit using Multisim.

# **ELEG 3063-P01**

## **Logic Circuits**

### **Project - Fall 2020**

#### **Objective**

The objective for this project is to design a circuit that functions as an 8 to 3 encoder when an enable input is set to 1 and as an 8x1 multiplexer when the enable line is set to zero. All of this can be implemented by using Multisim or an FPGA.

#### **Theories**

##### **Encoder**

An encoder is a combinational circuit that converts binary information from "n" input lines to a max of "2n" unique output lines for the purpose of making the circuit simpler.

##### **Multiplexer**

A multiplexer is a device that selects one of several digital input signals and sends those inputs to the final output. A multiplexer of 2n inputs allows the "n" select lines to be used to select the number of input lines to send to the final output.

#### **Project Requirements**

1. Design the circuit, specify the components, test the circuit in the laboratory and confirm the circuit operates as required.
  - a. Create a truth table for an 8 to 3 encoder with enable.
  - b. Create an 8 to 1 multiplexer.
  - c. Connect the 8 to 3 encoder to the 8 to 1 multiplexer. The two devices utilize the same eight input data lines.
  - d. Test the circuit for the correct operation.
2. Confirm with the circuit operation with the instructor.
3. Write a project report that include the following sections:
  - a. Introduction,
  - b. Circuit designs for each of the individual circuits and the combined circuit, including all truth tables,
  - c. Confirmation that the circuit operated as specified, and
  - d. Conclusion.
4. Indicate in your report the amount of work done by each member of your group. Signatures of the members in your group indicating they participated in the project as required.
5. Submit a hardcopy of the project report to the instructor by November 20, 2020 no later

than 12:00 noon.

**ABOVE AVERAGE**

**PRAIRIE VIEW A&M UNIVERSITY**  
**DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING**  
**LOGIC CIRCUITS – ELEG 3063 PO-I**  
**RUBRICS FOR GRADING DESIGN PROJECT**  
**FALL 2020**

**GROUPNUMBER:**

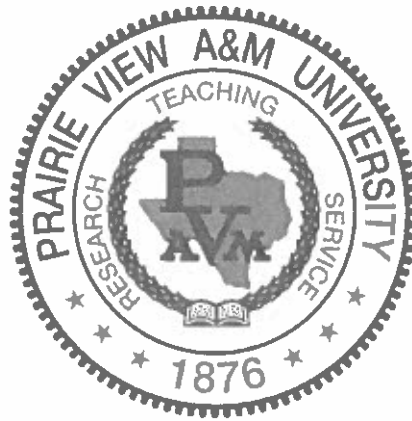
1

**GROUP MEMBERS:**

1. Dalton Jorge
2. John Barrett
3. Wesley Ponder
4. Michael Shepard

**RUBRICS FOR GRADING DESIGN PROJECT**

| ITEMS                                                                                                                                                                                                                                                                              | POINTS<br>ACHIEVED | MAXIMUM<br>POINTS |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------------------|
| 1. <i>Circuit was built and met design specifications</i> <ul style="list-style-type: none"> <li>Technical specifications were met.</li> <li>Design was checked by the instructor</li> </ul>                                                                                       | 30                 | 30                |
| 2. <i>Introduction</i>                                                                                                                                                                                                                                                             | 5                  | 5                 |
| 3. <i>Circuit Design</i> <ul style="list-style-type: none"> <li>Truth Tables</li> <li>Calculations and Simulations, if applicable</li> </ul>                                                                                                                                       | 10                 | 10                |
| 4. <i>Develop Procedure to Verify the Designed Circuit (Student Outcome 6.1)</i> <ul style="list-style-type: none"> <li>Identify parameters to be verified,</li> <li>Provide the steps for setting up and conducting the experiment</li> </ul>                                     | 10                 | 10                |
| 5. <i>Conduct Experiment (Student Outcome 6.2)</i> <ul style="list-style-type: none"> <li>Conduct verification while maintaining safety precautions</li> <li>Collect the data needed to show that your designed circuits meet the design specifications and constraints</li> </ul> | 15                 | 15                |
| 6. <i>Analysis and Interpretation of Experimental Results</i> <ul style="list-style-type: none"> <li>Present your data in tabular form to aid interpretation.</li> <li>Use the appropriate statistical method to analyze and interpret data, if necessary</li> </ul>               | 15                 | 15                |
| 7. <i>Discussion of Results and Conclusions (Student Outcome 6.3)</i> <ul style="list-style-type: none"> <li>Draw appropriate conclusions and recommendations using engineering judgement.</li> </ul>                                                                              | 10                 | 10                |
| 8. <i>General Write-up of Report</i> <ul style="list-style-type: none"> <li>Grammar and Adequacy of plots and figures</li> <li>Proper labeling of tables</li> <li>Proper references to tables</li> <li>Clear and meaningful sentences</li> </ul>                                   | 5                  | 5                 |
| 9. <i>Composite Report Grade</i>                                                                                                                                                                                                                                                   | 100                | 100               |
| 10. <i>Grade for Student Outcome 6 (Items #4, 5, 6, and 7)</i>                                                                                                                                                                                                                     |                    | 50                |
| 11. <i>Grade for Student Outcome 6 (Normalized to 100%)</i>                                                                                                                                                                                                                        |                    | 100               |



**Department of Electrical and Computer Engineering  
Prairie View A&M University**

**Course Name: Logic Circuits  
Course #: ELEG 3063  
Group #1**

**Project - Fall 2020**

**Group Members:**

Dalton Jorge  
John Barrett  
Wesley Ponder  
Michael Shepard

**Instructor: Dr. StJulian**

**Date of Submission: 11/20/2020**

## TABLE OF CONTENTS

|                       | Page |
|-----------------------|------|
| LIST OF FIGURES ..... | 2    |
| LIST OF TABLES .....  | 3    |
| INTRODUCTION .....    | 4    |
| CIRCUIT DESIGN .....  | 5    |
| TRUTH TABLE<br>.....  | 7    |
| MULTISIM DESIGN ..... | 8    |
| CONCLUSION .....      | 10   |
| CONTRIBUTION .....    | 11   |

## LIST OF FIGURES

|                                    | Page |
|------------------------------------|------|
| Fig. 1: MUX Output Test .....      | 8    |
| Fig. 2: 8x3 Decoder Output 0 ..... | 8    |
| Fig. 3: 8x3 Decoder Output 1 ..... | 9    |
| Fig. 4: 8x3 Decoder Output 2 ..... | 9    |

## LIST OF TABLES

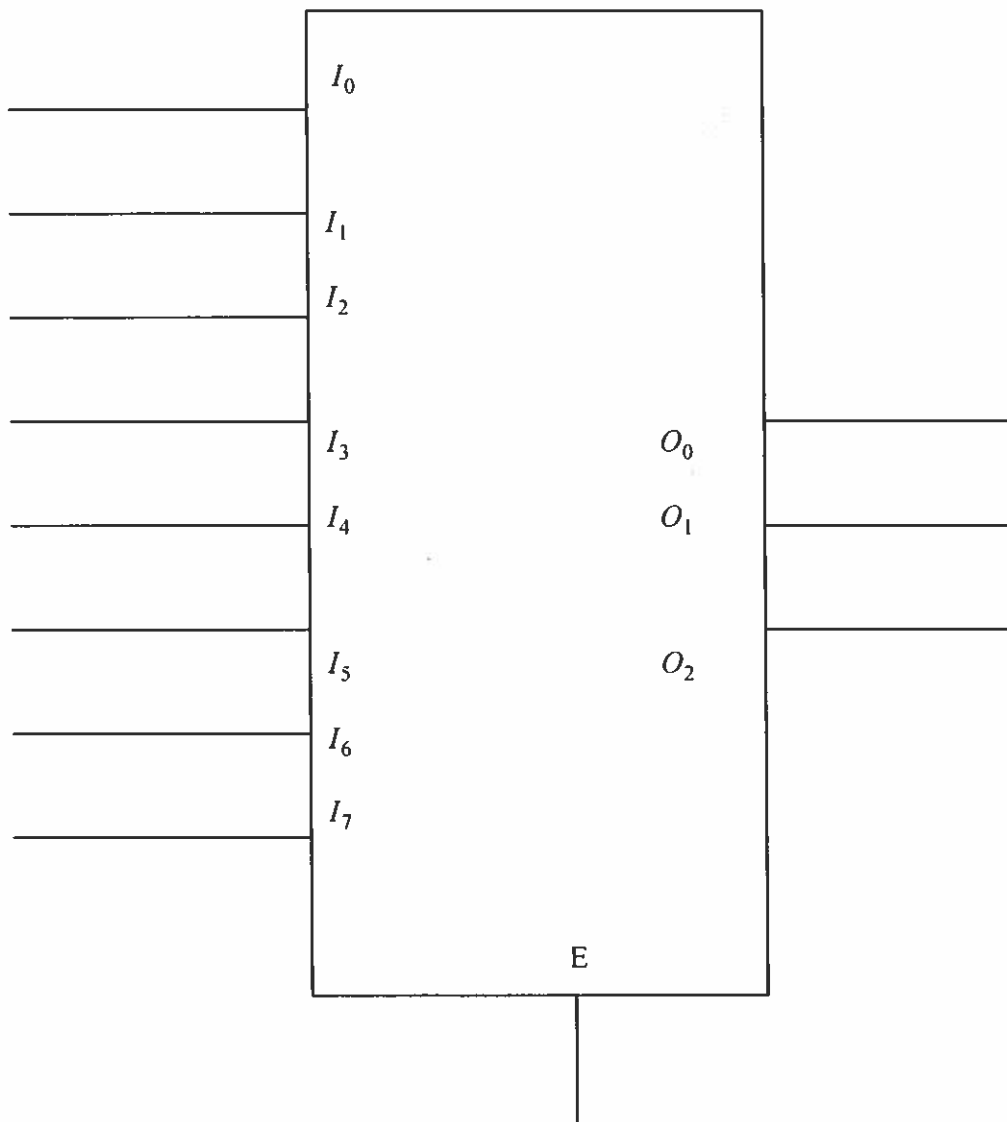
|                          | <b>Page</b> |
|--------------------------|-------------|
| Table: 8x3 Encoder ..... | 7           |
| Table: 8x1 MUX .....     | 7           |

## **Introduction**

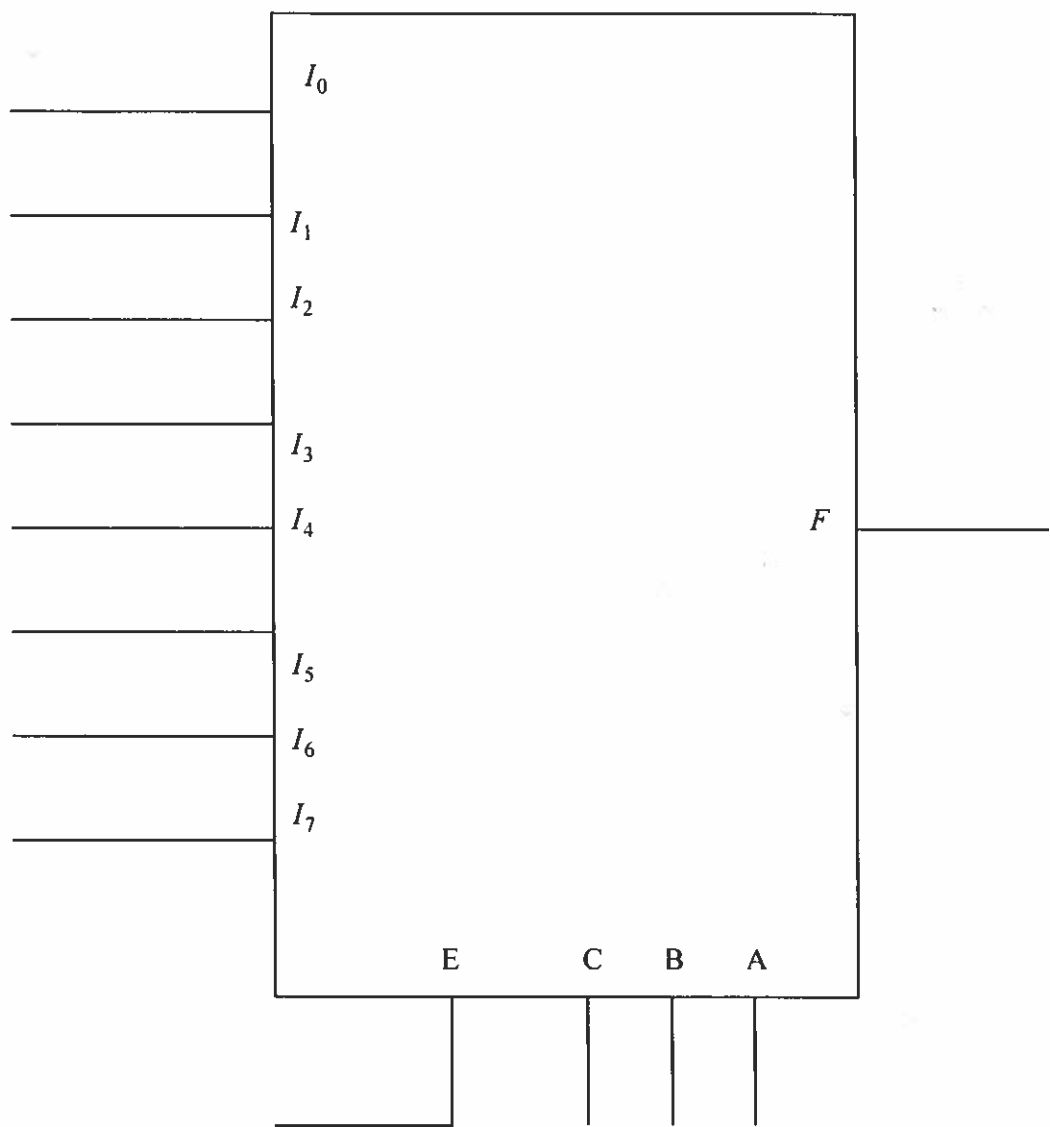
The project reflects the knowledge of encoders and multiplexers. The circuit functions as an 8x3 encoder when an enable input is set to 1 and an 8x1 multiplexer when the enable line is set to 0. An encoder is a device that converts an active input signal into a coded output signal. An encoder is a combinational component that converts binary information from "2<sup>n</sup>" input lines to a max of "n" unique output lines for the purpose of making the circuit simpler. A multiplexer is a device that selects one of several digital input signals and sends those inputs to the final output. This line switching has proven useful in certain devices to increase the amount of data that can be sent over a network. In this project, we used Multisim to build the circuit shown on pages 8 and 9. We crafted a truth table for the 8 to 3 encoder and also for an 8 to 1 multiplexer with a corresponding truth table. The 8 to 3 encoder is connected to the 8 to 1 multiplexer or mux. We saw the results for each part and lastly tested the circuit for any bugs or running issues.

**Circuit Design Examples:**

Encoder  
(8x3)



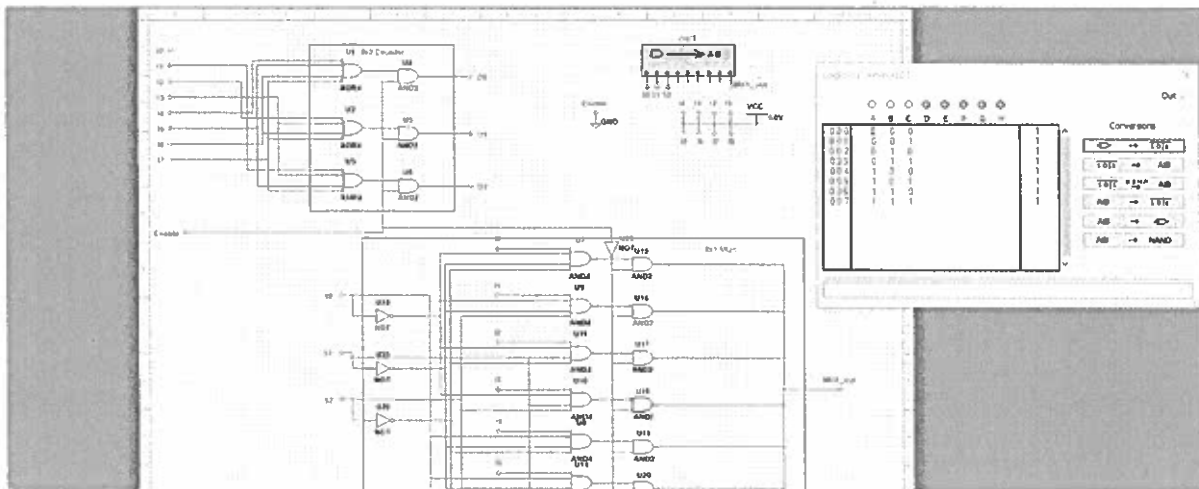
Multiplexer  
(8x1)



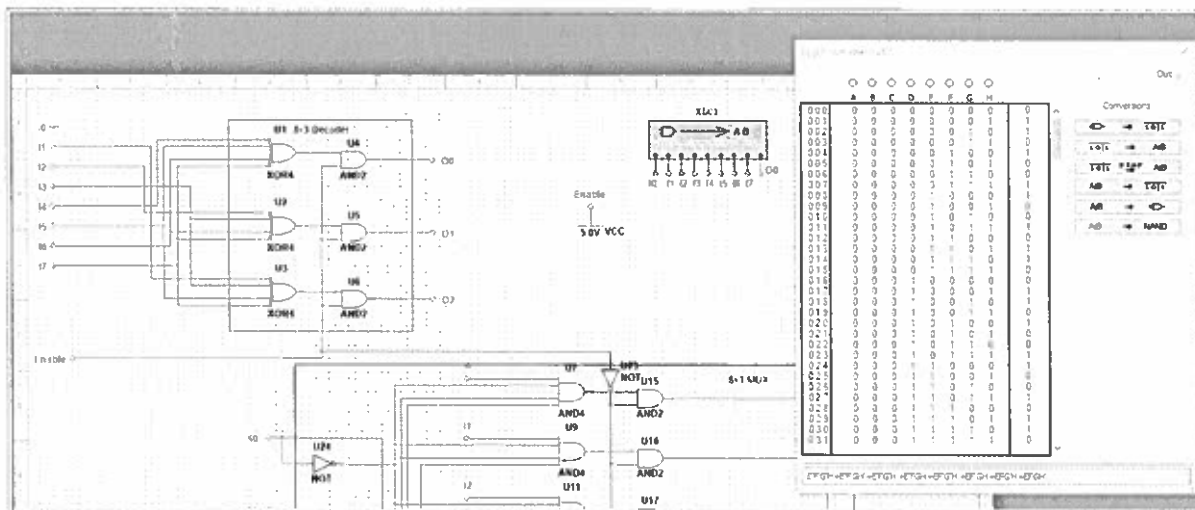
### Truth Tables:

| 8x3 Encoder |         |         |         |         |         |         |         |         |          |          |          |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|----------|----------|----------|
| Inputs      |         |         |         |         |         |         |         |         | Outputs  |          |          |
| Enable      | Input 0 | Input 1 | Input 2 | Input 3 | Input 4 | Input 5 | Input 6 | Input 7 | Output 0 | Output 1 | Output 2 |
| 0           | x       | x       | x       | x       | x       | x       | x       | x       | 0        | 0        | 0        |
| 1           | 1       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0        | 0        | 0        |
| 1           | 0       | 1       | 0       | 0       | 0       | 0       | 0       | 0       | 0        | 0        | 1        |
| 1           | 0       | 0       | 1       | 0       | 0       | 0       | 0       | 0       | 0        | 1        | 0        |
| 1           | 0       | 0       | 0       | 1       | 0       | 0       | 0       | 0       | 0        | 1        | 1        |
| 1           | 0       | 0       | 0       | 0       | 1       | 0       | 0       | 0       | 1        | 0        | 0        |
| 1           | 0       | 0       | 0       | 0       | 0       | 1       | 0       | 0       | 1        | 0        | 1        |
| 1           | 0       | 0       | 0       | 0       | 0       | 0       | 1       | 0       | 1        | 1        | 0        |
| 1           | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 1       | 1        | 1        | 1        |

| 8x1 MUX |          |          |          |         |  |
|---------|----------|----------|----------|---------|--|
| Inputs  |          |          |          | Outputs |  |
| Enable  | Select 0 | Select 1 | Select 2 | Output  |  |
| 0       | 0        | 0        | 0        | Input 0 |  |
| 0       | 0        | 0        | 1        | Input 1 |  |
| 0       | 0        | 1        | 0        | Input 2 |  |
| 0       | 0        | 1        | 1        | Input 3 |  |
| 0       | 1        | 0        | 0        | Input 4 |  |
| 0       | 1        | 0        | 1        | Input 5 |  |
| 0       | 1        | 1        | 0        | Input 6 |  |
| 0       | 1        | 1        | 1        | Input 7 |  |
| 1       | X        | X        | X        | 0       |  |

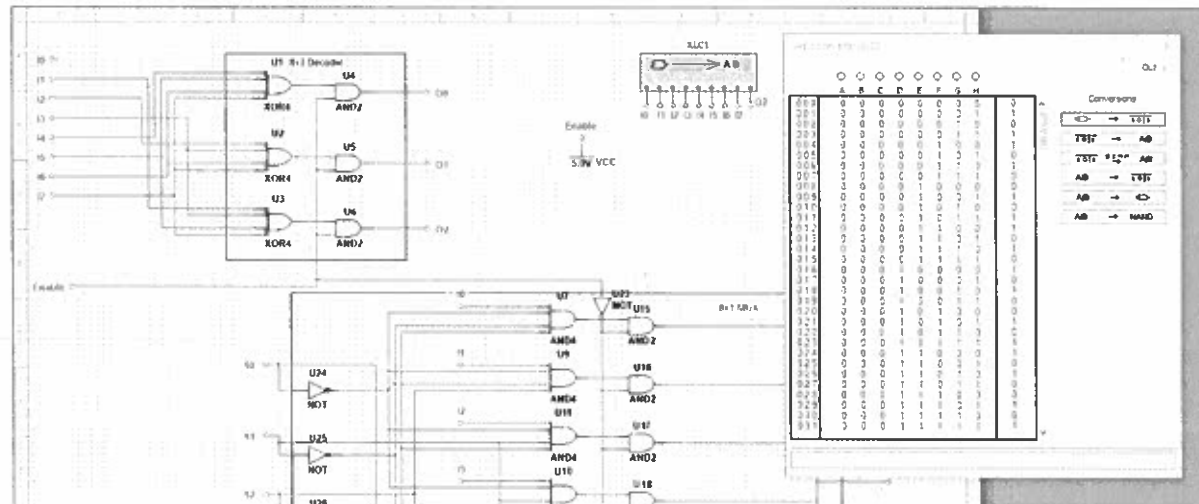
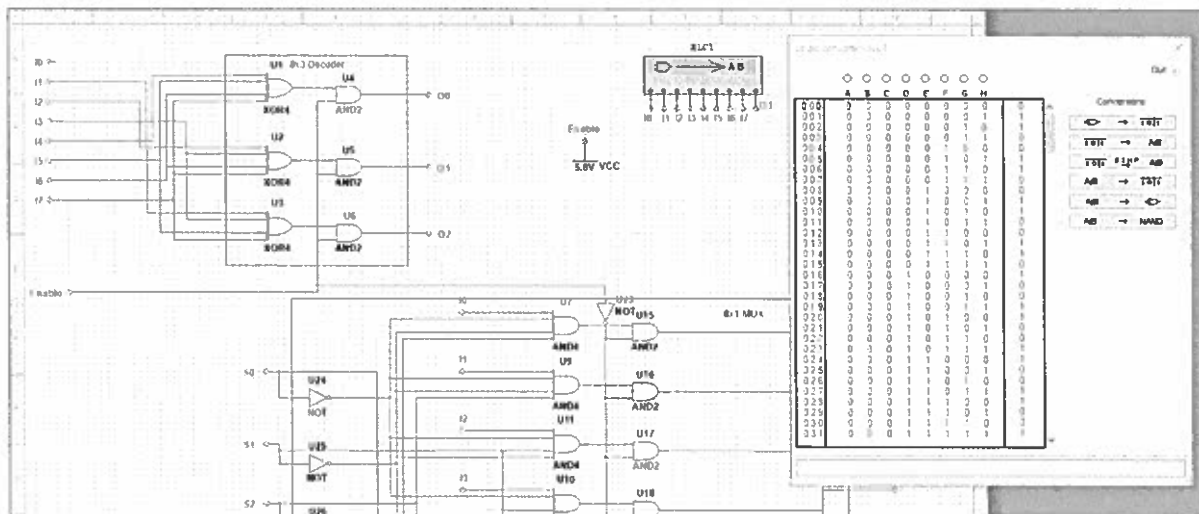


## Multisim Design:



MUX output test

8x3 Decoder Output 0



8x3 Decoder Output 1

8x3 Decoder Output 2

## **Conclusion**

In summation, we created the 8 to 1 multiplexer, which consisted of 8 data inputs and 1 output. The multiplexer has 3 select lines that determine which line is in use. We worked on creating the 8 to 3 encoder, where the encoder is connected to the multiplexer using an enabler and a NOT gate. A logic converter is connected to the cohesive circuit in order to show a truth table. Truth tables usually use binary values in order to show true and false, 1 for true and 0 for false. The multiplexer has one output as shown in the picture labeled as 'Multiplexer Output Test.' As you can see, there is a truth table response utilizing the logic converter. Each encoder output has its own corresponding truth table and responds differently. Each individual component of the circuit, whether that be the 8x1 multiplexer or the 8x3 encoder, is able to work independently if the enable line is set to zero or 1.

## Contribution

The total percentage performed by the member of the group #1 is 100%.

Dalton Jorge: 33.3% of participation.

Responsible to create the circuit design and  
the report

*Dalton Jorge*

Signed on 11/17/2020

John Barrett: 33.3% of participation.

Responsible to build the circuit on multisim  
And create the truth table

*John W Barrett*

Signed on 11/17/2020

Wesley Ponder: 33.3% of participation.

Responsible analyze the final data and finalize the  
report

*Wesley Ponder*

Signed on 11/18/2020

Michael Shepard: 0% of participation.

\_\_\_\_\_

## AVERAGE

**PRAIRIE VIEW A&M UNIVERSITY**  
**DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING**  
**LOGIC CIRCUITS – ELEG 3063 PO-I**  
**RUBRICS FOR GRADING DESIGN PROJECT**  
**FALL 2020**

**GROUPNUMBER:** 3

**GROUP MEMBERS:**

1. Arthur Quinny
2. Isaiah Allen
3. Ben Ombura
4. Hillel Lands

**RUBRICS FOR GRADING DESIGN PROJECT**

| ITEMS                                                                                                                                                                                                                                                                              | POINTS ACHIEVED | MAXIMUM POINTS |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------|
| 1. <i>Circuit was built and met design specifications</i> <ul style="list-style-type: none"> <li>Technical specifications were met.</li> <li>Design was checked by the instructor</li> </ul> <i>encoder requested priority encoder presented</i>                                   | 25              | 30             |
| 2. <i>Introduction</i>                                                                                                                                                                                                                                                             | 5               | 5              |
| 3. <i>Circuit Design</i> <ul style="list-style-type: none"> <li>Truth Tables</li> <li>Calculations and Simulations, if applicable</li> </ul>                                                                                                                                       | 5               | 10             |
| 4. <i>Develop Procedure to Verify the Designed Circuit (Student Outcome 6.1)</i> <ul style="list-style-type: none"> <li>Identify parameters to be verified,</li> <li>Provide the steps for setting up and conducting the experiment</li> </ul>                                     | 10              | 10             |
| 5. <i>Conduct Experiment (Student Outcome 6.2)</i> <ul style="list-style-type: none"> <li>Conduct verification while maintaining safety precautions</li> <li>Collect the data needed to show that your designed circuits meet the design specifications and constraints</li> </ul> | 15              | 15             |
| 6. <i>Analysis and Interpretation of Experimental Results</i> <ul style="list-style-type: none"> <li>Present your data in tabular form to aid interpretation.</li> <li>Use the appropriate statistical method to analyze and interpret data, if necessary</li> </ul>               | 10              | 15             |
| 7. <i>Discussion of Results and Conclusions (Student Outcome 6.3)</i> <ul style="list-style-type: none"> <li>Draw appropriate conclusions and recommendations using engineering judgement.</li> </ul>                                                                              | 10              | 10             |
| 8. <i>General Write-up of Report</i> <ul style="list-style-type: none"> <li>Grammar and Adequacy of plots and figures</li> <li>Proper labeling of tables</li> <li>Proper references to tables</li> <li>Clear and meaningful sentences</li> </ul>                                   | 5               | 5              |
| 9. <i>Composite Report Grade</i>                                                                                                                                                                                                                                                   | 85              | 100            |
| 10. <i>Grade for Student Outcome 6 (Items #4, 5, 6, and 7)</i>                                                                                                                                                                                                                     |                 | 50             |
| 11. <i>Grade for Student Outcome 6 (Normalized to 100%)</i>                                                                                                                                                                                                                        |                 | 100            |

*hooking truth table for mux*

Arthur Quinney  
Isaiah Allen  
Ben Ombura  
Hillel Lands

**ELEG 3063 – P01**  
**LOGIC CIRCUITS**  
**PROJECT – FALL 2020**

Today's objective is to enlighten the reader on how to design a circuit that will function as an 8 to 3 encoder when an enabler input is set to 1. We are to also demonstrate with an 8 x 1 multiplexer when the enabler is set to 0. By utilizing a Windows-based schematic capture and stimulation application (Multisim) the user will capture and simulate this design when these two devices utilize the same eight input data lines.

The encoder is a combinational circuit design which operates with binary quantities. When utilizing the binary quantities, "on" and "off" will represent 1 and 0 which signifies (true or false). This is known to be the logic of Boolean algebra. Diagram: Truth table will consist of 8 input lines and 3 output lines. Please see truth table below for this encoder circuit. As values are numerically changed within the input and output lines according to the truth table the test circuit you can see that the simulation is positive.

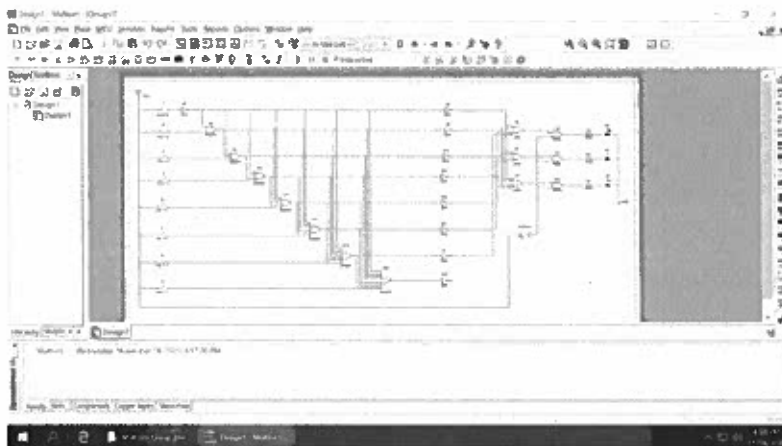
Truth Table for 8 to 3 Encoder

| A | B | C | D | E | F | G | H | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|---|---|---|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     | 0     | 0     |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0     | 0     | 1     |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0     | 1     | 0     |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0     | 1     | 1     |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1     | 0     | 0     |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1     | 0     | 1     |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1     | 1     | 0     |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1     | 1     | 1     |

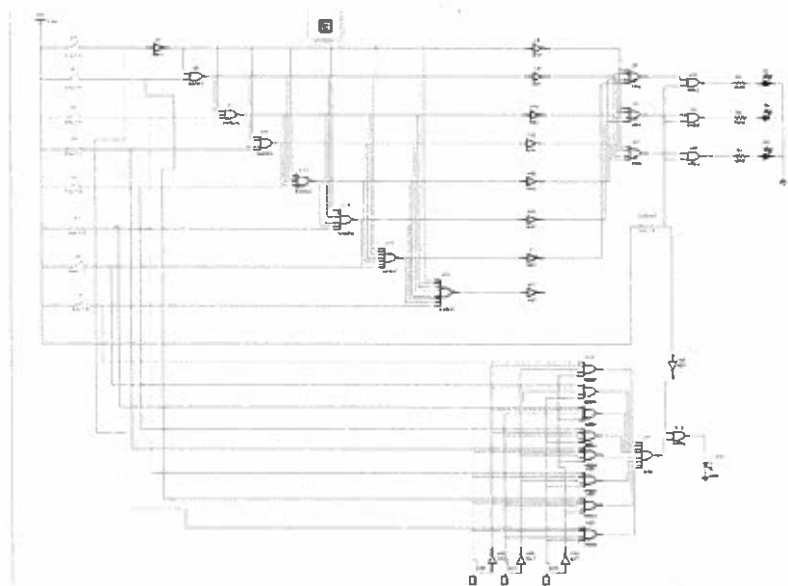
$Q_2 = G + E + C + A + E_n = 4$

Arthur Quinney  
Isaiah Allen  
Ben Ombura  
Hillel Lands

The 8x3 encoder works by the needed outputs turning on when their related inputs are activated. In a truth table the higher priority input will be more likely to be shown and the lower priority input will be less likely to be shown so this reflects which output will be shown as a result. The output will be shown using binary values written in the truth table.



A NOT gate and enabler were used to connect the 8 by 3 encoder to the 8 by 1 multiplexer. There are switches connected also in order to make the circuit work cohesively and show correct output ramification. In order to make the circuit work both the encoder and the mux had to work and show outputs independently from each other.



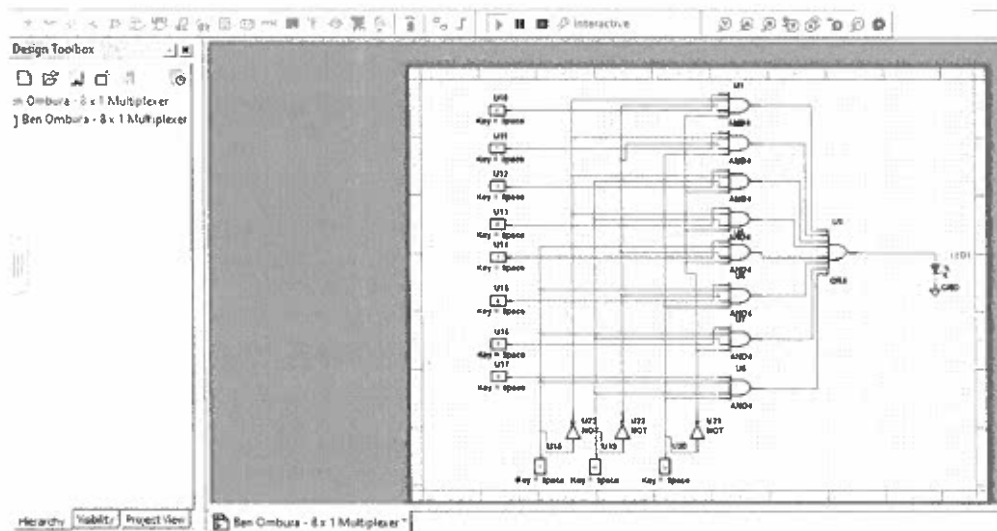
Arthur Quinney  
Isaiah Allen  
Ben Ombura  
Hillel Lands

In the 8 x 1 multiplexer, we used interactive digital constant components as inputs that work like switches. The interactive digital constants can be switched from 0 to 1. Switching to 1 produces a strong digital high state and switches to 0 produces a low digital state within the circuit. We connected all the inputs to an AND gate, which connected to an OR gate output. The switch combinations that work to turn on the LED are listed

U20: switched to 1, U11: switched to 1

U19: switched to 1, U12: switched to 1

U18: switched to 1, U14: switched to 1



When utilizing Multisim to perform tests, we see that the outcome was a successful operation. The circuits were designed based on the outline instructions. The encoder and multiplexer were tested to show correctness and precision. Each had its outputs displayed in the truth table as you can see in then pictures. In conclusion, the circuit can run in a tenacious or self-sufficient manner.

Arthur Quinney  
Isaiah Allen  
Ben Ombura  
Hillel Lands

Responsible for overseeing all pertinent documents and analyzing the final data to create the report.

Arthur Quinney

Created the 8 X 1 Multiplexer and performed all tests to ensure operational functionality

Ben Ombura

Created the 8 X 3 Encoder and performed all tests to ensure its operational functionality

Isaiah Allen

Constructed and combined both circuits and oversaw its operational functionality.

Hillel Lands

**BELOW AVERAGE**

**PRAIRIE VIEW A&M UNIVERSITY**  
**DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING**  
**LOGIC CIRCUITS – ELEG 3063 PO-I**  
**RUBRICS FOR GRADING DESIGN PROJECT**  
**FALL 2020**

**GROUPNUMBER:**

8

**GROUP MEMBERS:**

1. Alyssa Reed

2. Osesiye Ayeni

3. Jacqueline Torralba

4. Christopher Rollerson

**RUBRICS FOR GRADING DESIGN PROJECT**

| ITEMS                                                                                                                                                                                                                                                                              | POINTS ACHIEVED | MAXIMUM POINTS |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------|
| 1. <i>Circuit was built and met design specifications</i> <ul style="list-style-type: none"> <li>Technical specifications were met.</li> <li>Design was checked by the instructor</li> </ul>                                                                                       | 20              | 30             |
| 2. <i>Introduction</i>                                                                                                                                                                                                                                                             | 5               | 5              |
| 3. <i>Circuit Design</i> <ul style="list-style-type: none"> <li>Truth Tables</li> <li>Calculations and Simulations, if applicable</li> </ul>                                                                                                                                       | 5               | 10             |
| 4. <i>Develop Procedure to Verify the Designed Circuit (Student Outcome 6.1)</i> <ul style="list-style-type: none"> <li>Identify parameters to be verified,</li> <li>Provide the steps for setting up and conducting the experiment</li> </ul>                                     | 10              | 10             |
| 5. <i>Conduct Experiment (Student Outcome 6.2)</i> <ul style="list-style-type: none"> <li>Conduct verification while maintaining safety precautions</li> <li>Collect the data needed to show that your designed circuits meet the design specifications and constraints</li> </ul> | 0               | 15             |
| 6. <i>Analysis and Interpretation of Experimental Results</i> <ul style="list-style-type: none"> <li>Present your data in tabular form to aid interpretation.</li> <li>Use the appropriate statistical method to analyze and interpret data, if necessary</li> </ul>               | 8               | 15             |
| 7. <i>Discussion of Results and Conclusions (Student Outcome 6.3)</i> <ul style="list-style-type: none"> <li>Draw appropriate conclusions and recommendations using engineering judgement.</li> </ul>                                                                              | 10              | 10             |
| 8. <i>General Write-up of Report</i> <ul style="list-style-type: none"> <li>Grammar and Adequacy of plots and figures</li> <li>Proper labeling of tables</li> <li>Proper references to tables</li> <li>Clear and meaningful sentences</li> </ul>                                   | 5               | 5              |
| 9. <i>Composite Report Grade</i>                                                                                                                                                                                                                                                   | 63              | 100            |
| 10. <i>Grade for Student Outcome 6 (Items #4, 5, 6, and 7)</i>                                                                                                                                                                                                                     |                 | 50             |
| 11. <i>Grade for Student Outcome 6 (Normalized to 100%)</i>                                                                                                                                                                                                                        |                 | 100            |

Not truth table?



# **Project Report**

**ELEG 3063-P01**

**Fall 2020**

## **Group 8**

**Alyssa Reed**

**Osesiye Ayeni**

**Jacqueline Torralba**

**Christopher Rollerson**

**Submission Date: 11/20/2020**

**Department of Electrical and Computer Engineering  
Prairie View A&M University**

## Introduction:

Our group consists of 4 students whose objective is to design a circuit that functions as an 8x3 encoder when an enable input is set to 1 and as an 8x1 multiplexer when set to 0. We will be demonstrating our knowledge and capabilities using the MultiSim software. After our circuit is designed and has been tested and proven to operate properly, we must then present our design to the professor then create a report that adequately demonstrates and explains all that we have done and learned.

## Circuit Design:

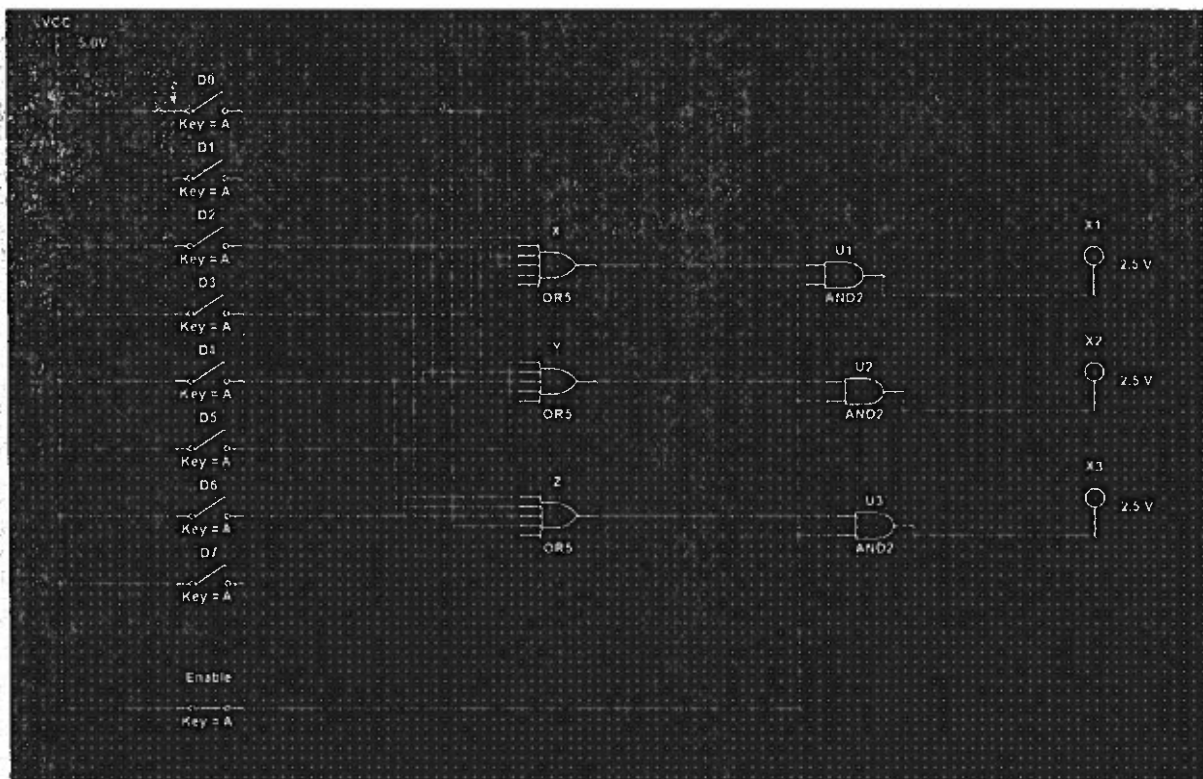


Figure 1: 8x3 Encoder

| <u>D0</u> | <u>D1</u> | <u>D2</u> | <u>D3</u> | <u>D4</u> | <u>D5</u> | <u>D6</u> | <u>D7</u> | <u>X</u> | <u>Y</u> | <u>Z</u> |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|----------|
| 1         | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 1        | 1        | 1        |
| 0         | 1         | 0         | 0         | 0         | 0         | 0         | 0         | 1        | 1        | 0        |
| 0         | 0         | 1         | 0         | 0         | 0         | 0         | 0         | 1        | 0        | 1        |
| 0         | 0         | 0         | 1         | 0         | 0         | 0         | 0         | 1        | 0        | 0        |
| 0         | 0         | 0         | 0         | 1         | 0         | 0         | 0         | 0        | 1        | 1        |
| 0         | 0         | 0         | 0         | 0         | 1         | 0         | 0         | 0        | 1        | 0        |
| 0         | 0         | 0         | 0         | 0         | 0         | 1         | 0         | 0        | 0        | 1        |
| 0         | 0         | 0         | 0         | 0         | 0         | 0         | 1         | 0        | 0        | 0        |

Figure 2: Truth Table for 8x3 encoder:

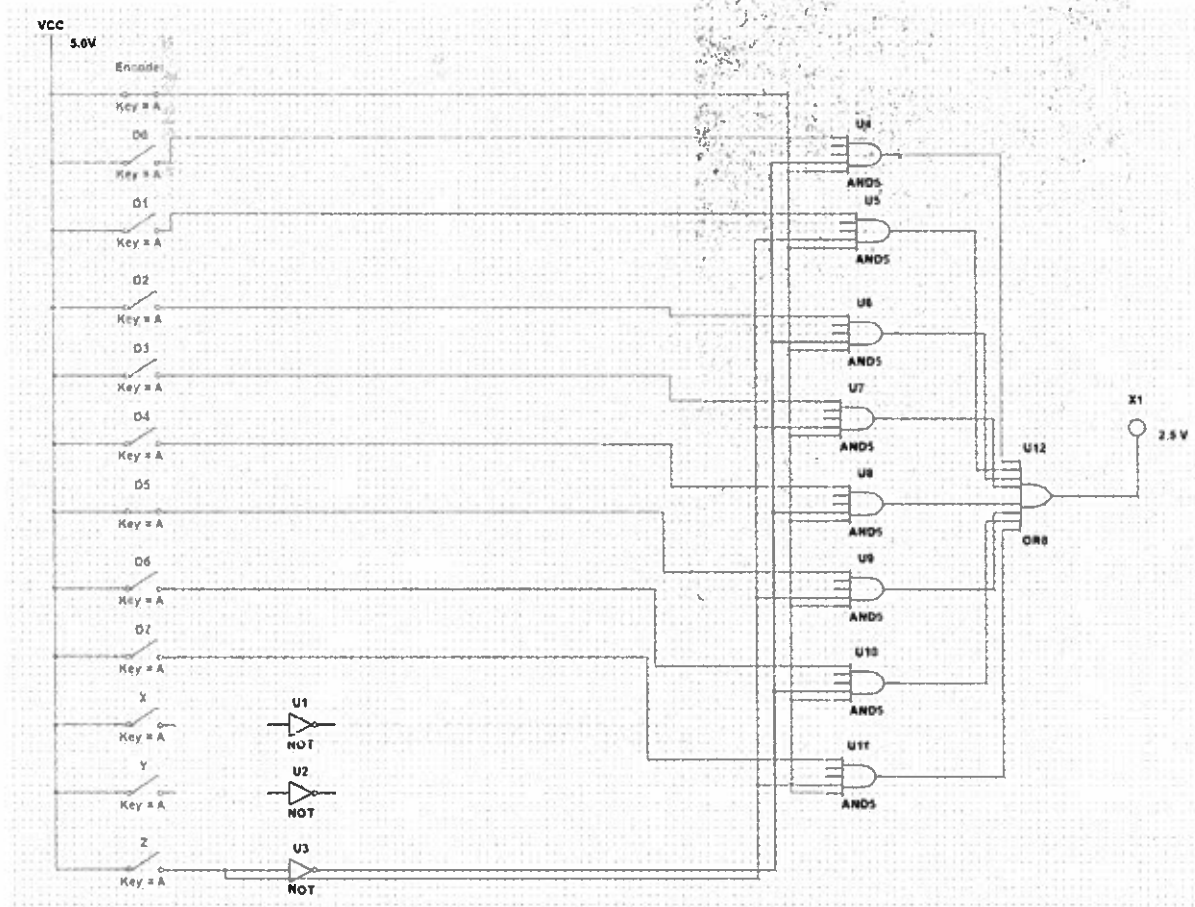


Figure 3: 8x1 Mux

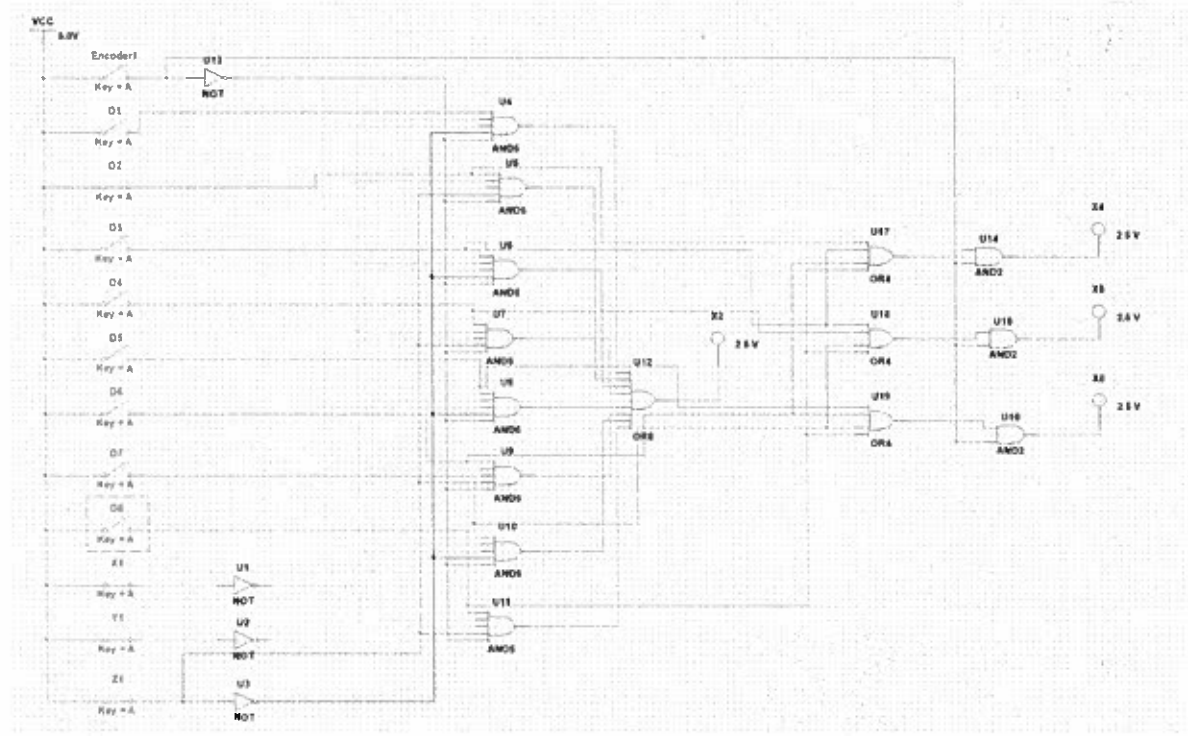


Figure 4: Combined Encoder and Mux

#### Confirmation of designed circuit operations (Analysis):

In figure 1 we have the 8 by 3 encoder, that can be identified with 8 different inputs, and 3 different outputs. This encoder is valid with the  $2^n = \text{input to } n = \text{output}$  rule, since  $2^3=8$ .

This 8 by 3 encoder is composed of AND, and OR logic gates. There is a supply VCC power source, and switches attached to the 8 by 3 encoder that will help us identify the outputs known as single binary codes. These single binary codes from the outputs are seen in figure 2 which is the respective truth table for the 8 by 3 encoder or figure 1. The last characteristic to discuss in figure 1 is the enabler that is seen as the last switch on the bottom left of the logic circuit diagram labeled “enable”, this enabler allows the encoder to be turned on and off. There are two types of enablers known as active high and active low, in this case we have an active high enable, where when  $E (\text{enable}) = 1$ , it turns on, when  $E = 0$  it is off.

In figure 2 as discussed previously is the truth table for the 8 by 3 encoder, only one input has a value of 1 at any given time and the Boolean functions are displayed below for the 8 by 3 encoder truth table.

$$X = D0 + D1 + D2 + D3$$

$$Y = D0 + D1 + D4 + D5$$

$$Z = D0 + D2 + D4 + D6$$

In figure 3 we have an 8 by 1 multiplexer, also known as data selectors, that act as digitally controlled switches. This will at the end be connected to the 8 by 3 encoder creating a connected encoder to multiplexer. These logic circuits are both combinational logic devices that create a final circuit where the 8 by 3 encoder will have the enable set to 1, while at the same time an 8 by 1 multiplexer is enabled to 0 and was successfully done as seen above in figure 4.

### **Conclusion:**

In conclusion, by using MultiSim, we successfully created a circuit that functions as an 8 to 3 encoder when an enable input is set to 1 and as an 8 x 1 multiplexer when the enable line is set to 0. In creating the truth table, we had to include a VCC power source and switches to attach to an 8x3 encoder with enable then connected the circuit built to a logic converter to access the truth table. With the help of our active high enabler when  $E = 1$ , the encoder turned on and when  $E = 0$  it turned off.

**Appendix:**

This report was designed by Alyssa and edited by the entire team. The introduction was done by Alyssa. The circuit design and everything incorporated into that section was completed by Christopher. The confirmation of the designed circuit operations section was completed by Jacqueline and the conclusion was done by Osesiye.

Signatures:

X Alyssa D. Reed

X Christopher Rollerson

X Osesiye Ayeni

X Jacqueline Torralba