

**ROY G. PERRY COLLEGE OF ENGINEERING
ELECTRICAL AND COMPUTER
ENGINEERING DEPARTMENT
PRAIRIE VIEW A&M UNIVERSITY**

ASSESSMENT REPORT COVER PAGE

ELEG 2311-001 LOGIC CIRCUITS

SPRING 2022 SEMESTER

NAME OF INSTRUCTOR: H. St. Julian

Revised: 08/05/2019

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 - 6.0 An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgement to draw conclusions.

Detailed Course Syllabus
(Distributed to Students at the beginning of the Semester)

Course Description in ABET Format

ELEG 2311 Logic Circuits

1.	Course number and name:	ELEG 2311 – Logic Circuits
2.	Credits and contact hours:	3 credit hours
3.	Instructor's or course coordinator's name:	H. St. Julian
4.	Text book: Title:	Digital Design
	Author:	M. Morris Mano and Michael D. Ciletti
	Publisher, Year & Edition:	Pearson Education, Inc, 2018, 6 th Edition
	a. Other Supplemental material	Logic and Computer Design Fundamentals, 3 rd Edition, Morris Mano and Charles Kime
5.	Specific course information	
	a. Brief description of the content of the course (catalog description)	Number systems and codes. Boolean algebra and logic minimization methods. Combinational and sequential design using logic gates and flip flops. Computer-aided design tools for digital design, simulation, and testing.
	b. Prerequisites or Co-requisites	MCEG 3013 Heat Transfer MCEG 3023 Thermodynamics II None
	c. *Indicate whether a required, elective, or selected elective (as per definition provided) course in the program	Required
6.	Specific goals for the course	Students will be able to :
	a. Specific outcomes of instruction (e.g. the student will be able to explain the significance of current research about a particular topic.)	1. understand the operation of basic logic components 2. understand the detail steps of the design process including problem formulation, logic optimization, technology mapping to NAND and NOR gates 3 design combinational logic circuits using multiplexer, decoders, comparators and adders 4. understand synchronous sequential logic analysis and design, basic latches, flip flops, clocking and timing diagrams 5. use Hardware Description Language (HDL), such as Verilog
	b. Explicitly indicate which of the student outcomes listed in Criterion	This course addresses:

	3 or any other outcomes are addressed by the course.	Outcome 6 Ability to develop and conduct appropriate experimentation, analyze and interpret data and use engineering judgement to draw conclusions.
7	Brief list of topics to be covered	Digital Systems and Binary Numbers Boolean Algebra and Logic Gates Gate Level Minimization Combinational Logic Synchronous Sequential Logic Registers and Counters

Additional Course Syllabus Information

CLASS HOURS: 8:00-9:20 AM TTH
CLASS ROOM: ROOM: 139 NENGR
OFFICE: Rm 349 NENGR
OFFICE HOURS: AS POSTED

CLASS PUNCTUALITY:

The class roll will be checked within the first five minutes of the class period. Anyone who comes in after the roll is checked will be considered late.

CHEATING AND PLAGIARISM

Students are referred to the University Policy about cheating and plagiarism. It shall be the policy in this course to discourage cheating to the extent possible, rather than to try to trap and to punish. On the other hand, in fairness to all concerned, **cheating and plagiarism will be treated severely wherever it is found.**

Because a large part of the learning experience comes from interaction with your peers, students are encouraged to discuss assignments with each other. The material submitted for grading must, however, be the product of individual or assigned group effort; anything else constitutes cheating.

DESIGN: This is a design course and students will be put into design groups. Group dynamics will be very important. Each group of students will be given a design project which will require the basic knowledge of combinational logic circuits. A systematic approach to the design process will be essential.

REPORTS:

The final project report should be completely typed in a formal report format and the operation of the project demonstrated to the professor.

PROJECT ASSIGNMENT:

The project report should be handed in on the due date. You may submit them typed or neatly handwritten. Students are responsible for organizing themselves in order to complete the design project. Each student in the group shall be responsible for any and all details of the design project.

Class Attendance Policy

Prairie View A&M University requires regular class attendance. Attending all classes supports full academic development of each learner whether classes are taught with the instructor physically present or via distance learning technologies such as interactive video. Excessive absenteeism, whether excused or unexcused, may result in a student's course grade being reduced or in assignment of a grade of "F". Absences are accumulated beginning with the first day of class during regular semesters and summer terms.

The sequencing of topics to be covered in this course has been carefully done to provide a logical transition from one topic to another. Each topic builds on the previous topics and students are encouraged to ensure thorough understanding of earlier topics to aid them to understand the new ones being introduced. The plan of course described below was designed with the above objectives in mind.

NOTE:

1. Please read the UNIVERSITY CLASS ATTENDANCE POLICY (undergraduate catalog, 2005-2007, pp. 111).
2. Please read the University Policy on Academic Honesty (undergraduate catalog, 2005-2007, pp. 111-116).

DISABILITY REQUIREMENTS:

Do you have any special needs in this class related to a disability? If yes, please contact your instructor as soon as possible. (Undergraduate Catalog, 2005-2007, p. 61) Any student who has, or believes they may have a disability that requires accommodations is advised to contact the Office of Students with Disabilities at 936-857-2610 in Evans Hall Room 315.)

Grading Matrix (Grading matrix may be changed at instructor's discretion, in which case all students will be informed).

Instrument	Value (percentages)
Exams (3 exams)	50% (16%,17%,17%)
Attendance, Quizzes and Project	25%
Homework (collected but not graded)	
Final Exam (Comprehensive)	25%
Total:	100%

Grade Determination:

A = 90% or better
B = 80– 89%
C = 70-79%
D = 60 – 69%
F = Less than 60%

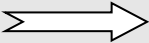
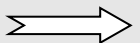
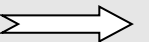
Tentative Course Schedule

Week	Description/Topic
1	Digital Systems; Binary, Octal, and Hexadecimal Numbers; Conversion From Decimal to Other Bases; Arithmetic Operations
2	Boolean Algebra; Basic Identities of Boolean Algebra; Algebraic Manipulation; Binary Logic and Gates; Timing Diagrams.
3, 4	Test 1 Karnaugh Map (K-map) Construction, Algebraic Manipulation vs K-map Simplification, Minterms and Maxterms, Sum-of- Products Simplification, Product-of-Sums Simplification, Don't Care conditions.
5	Exclusive-OR Gates, Odd Function, Parity Generation and Checking.
6	FPGA Programming, Combinational Logic Circuits, Analysis and Design Procedures, Derivation of Boolean Functions, Derivation of Truth Table, Logic Simulation.
7, 8	Decoders, Decoder Expansion, Combinational Circuit Implementation, Encoders, Priority Encoder.
9	Multiplexers, Combinational Circuit Implementation, Demultiplexer. Test 2
10	Binary Adders, Half Adder, Full Adder, Binary Ripple Carry Adder, Binary Adder-Subtractors.
11	Sequential Circuits vs Combinational Circuits, Flip-Flops, Input Equations, State Table, Analysis with JK Flip-Flops.
12	State Diagram, Excitation Table, Design Procedure, Sequential Circuit Design with Unused States.
13	Registers, Ripple Counter Test 3
14	Synchronous Binary Counters, BCD Counter, Arbitrary Count Sequence.
15	Random-Access Memory (RAM), Three-State Buffers, Coincident Selection, Array of RAM ICs Read-Only Memory, Programmable Logic Array, Programmable Array Logic Devices
16	Final Exam (Comprehensive)

END OF SEMESTER COURSE OUTCOME ASSESSMENT REPORT
ELEG 2311-001 LOGIC CIRCUITS
SPRING 2022 SEMESTER

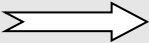
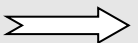
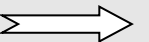
Report Prepared by: H. St. Julian

Report Date: June 14, 2022

Semester	Analysis Type	Number of Students	Outcome 6 An ability to develop an conduct experimentation, analyze and interpret data and use engineering judgement to draw conclusions			
			Expected Class Average/	Expected Percent of students at or above average	Class Average	% Students meeting Expected Average
Project – S22	Direct	35	75	70	86.7	92
Lecture – S22	Direct	35	75	70	72.48	73
Implementation Summary	Items implemented from previous report or after meeting previous instructor	A lectures on the design process covering this performance criteria were given and notes distributed to students.				
Perceived Problems	Perceived problems are directly related to the PC and the sub items under them 	A few students had problems identifying the design constraints and merging the encoder and multiplexer together and then enabling the appropriate circuit when necessary				
Plans for Addressing Problems	Plans for address specific measures to address PC and their sub areas 	The following is recommended for implementation: Distinction between design constraints and design requirements should be made clear to students.				
Overall Trend over Periods	Ascertain if there were improvements over previous semesters 	The students analyzed how to connect the different circuits and how to enable the various circuits according to the design constraints. Overall, the students did very well.				
Were Expectations Met?		YES				

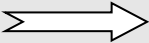
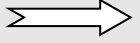
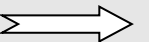
END OF SEMESTER COURSE OUTCOME ASSESSMENT REPORT
ELEG 2311-001 LOGIC CIRCUITS
SPRING 2022 SEMESTER

Report Prepared by: H. St. Julian
Report Date: June 14, 2022
Electrical Engineering

Semester	Analysis Type	Number of Students	Outcome 6 An ability to develop an conduct experimentation, analyze and interpret data and use engineering judgement to draw conclusions			
			Expected Class Average/	Expected Percent of students at or above average	Class Average	% Students meeting Expected Average
Spring 2022	Direct	28	75	70	75.9	61
Implementation Summary	Items implemented from previous report or after meeting previous instructor	A lectures on the design process covering this performance criteria were given and notes distributed to students.				
Perceived Problems	Perceived problems are directly related to the PC and the sub items under them 	A few students had problems identifying the design constraints and merging the encoder and multiplexer together and then enabling the appropriate circuit when necessary				
Plans for Addressing Problems	Plans for address specific measures to address PC and their sub areas 	The following is recommended for implementation: Distinction between design constraints and design requirements should be made clear to students.				
Overall Trend over Periods	Ascertain if there were improvements over previous semesters 	The students analyzed how to connect the different circuits and how to enable the various circuits according to the design constraints. Overall, the students did very well.				
Were Expectations Met?		YES				

END OF SEMESTER COURSE OUTCOME ASSESSMENT REPORT
ELEG 2311-001 LOGIC CIRCUITS
SPRING 2022 SEMESTER

Report Prepared by: H. St. Julian
Report Date: June 14, 2022
Computer Engineering

Semester	Analysis Type	Number of Students	Outcome 6 An ability to develop an conduct experimentation, analyze and interpret data and use engineering judgement to draw conclusions			
			Expected Class Average/	Expected Percent of students at or above average	Class Average	% Students meeting Expected Average
Spring 2022	Direct	7	75	70	59	29
Implementation Summary	Items implemented from previous report or after meeting previous instructor	A lectures on the design process covering this performance criteria were given and notes distributed to students.				
Perceived Problems	Perceived problems are directly related to the PC and the sub items under them 	A few students had problems identifying the design constraints and merging the encoder and multiplexer together and then enabling the appropriate circuit when necessary				
Plans for Addressing Problems	Plans for address specific measures to address PC and their sub areas 	The following is recommended for implementation: Distinction between design constraints and design requirements should be made clear to students.				
Overall Trend over Periods	Ascertain if there were improvements over previous semesters 	The students analyzed how to connect the different circuits and how to enable the various circuits according to the design constraints. Overall, the students did very well.				
Were Expectations Met?		YES				

ASSIGNMENTS FOR OUTCOME 6

An ability to develop and conduct appropriate experimentation, analyze and interpret data and use engineering judgement to draw conclusions.

ELECTRICAL & COMPUTER ENGINEERING OUTCOMES

SPECIFIC ASSIGNMENT COVER SHEET

ELEG 2311 Logic Circuits

SPRING 2022

Instructor: H. St. Julian

Title of Assignment

Design a circuit that functions as an 8 to 3 encoder when an enable bit is set to 1 and as an 8x1 multiplexer when the enable bit is set to zero.

Outcome Measured Using this Assignment

Outcome 6

An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions

Check the experimentation problem characteristics related to this assignment

Ability to develop experiment Requires students to	
X	Identify the appropriate parameters or variables and relationships (independent, dependent and control variables),
X	Identify and select appropriate equipment or components for measuring the parameters
X	Provide steps for setting up and conducting the experiment and
	Identify data collection method to support experiments (if needed)
Ability to conduct experiments Requires students to	
X	Conduct experiment while maintaining all safety precautions
X	Demonstrate knowledge of how to use the equipment safely
	Collect and record data using appropriate units of measurement and significant figures
Ability to analyze and interpret experimental data Requires students to	
X	Present the data (raw /derived) in tabular or graphical form to meet the objectives and to aid in interpretation
	Use appropriate statistical analysis methods to analyze and interpret data
	discuss the raw and derived data/graphs and assess the validity of the results
Demonstrate the use of engineering judgement in the development and analysis of the experiment Requires students to	
X	Draw appropriate conclusions and recommendations using engineering judgement.

Brief justification of the suitability of assignment for the outcome

After the students complete the paper design, they implement and test the circuit using Multisim.

ELEG 2311-P01

Logic Circuits

Project – Spring

2022

Objective

The objective for this project is to design a circuit that functions as an 8 to 3 encoder when an enable input is set to 1 and as an 8x1 multiplexer when the enable line is set to zero. All of this can be implemented by using Multisim or an FPGA.

Theories

Encoder

An encoder is a combinational circuit that converts binary information from "n" input lines to a maximum of "2n" unique output lines for the purpose of making the circuit simpler.

Multiplexer

A multiplexer is a device that selects one of several digital input signals and sends those inputs to the final output. A multiplexer of 2n inputs allows the "n" select lines to be used to select the number of input lines to send to the final output.

Project Requirements

1. Design the circuit, specify the components, test the circuit in the laboratory and confirm the circuit operates as required.
 - a. Create a truth table for an 8 to 3 encoder with enable.
 - b. Create an 8 to 1 multiplexer.
 - c. Connect the 8 to 3 encoder to the 8 to 1 multiplexer. The two devices utilize the same eight input data lines.
 - d. Test the circuit for the correct operation.
2. Confirm with the circuit operation with the instructor.
3. Write a project report that include the following sections:
 - a. Introduction,
 - b. Circuit designs for each of the individual circuits and the combined circuit, including all truth tables,
 - c. Confirmation that the circuit operated as specified, and
 - d. Conclusion.
4. Indicate in your report the amount of work done by each member of your group.
Signatures of the members in your group indicating they participated in the project as

required.

5. Submit a hardcopy of the project report to the instructor by April 21, 2022 no later than 12:00 noon.