**Digital Systems Preliminary Examination Fall 2017**

1. Simplify the following Boolean function using a K-map.

F(W,X,Y,Z) = ∑(0,1,2,3,4,5,10)

D = ∑(6,14), where D is a don’t care condition.

1. Design a sequential counter which counts the following sequence in the order listed: (0, 2,4,6,7,0). The sequence starts at zero and ends at zero. Implement with a T- flip flop or a D- flip flop. Specify the flip flop you will use.
2. Illustrate the State Table
3. Illustrate the State Diagram
4. Draw the sequential Circuit.
5. Implement the following functions:

F1 = ABC’ + AC + A’B’C’

F2 = A’B’C + BC

Using:

1. A Programmable Logic Array(PLA)
2. A Programmable Array Logic (PAL) device
3. Explain the fundamental differences between the RAM and ROM memory modules.
4. Design a 2 to 4 decoder using basic elements: (AND, OR, INVERTER gates, etc).
5. Design a 4 to 1 multiplexer to implement the function: f(x,y,z)= ∑(1,2,6,7). You may use a block to represent the multiplexer, with the appropriate inputs, selection lines, and output. Illustrate the Truth Table for the implementation.
6. Perform the following binary subtraction of unsigned numbers using two’s complement. Show your work. 111010 - 001010.