**Digital Systems Preliminary Examination Spring 2016**

1. Simplify the following Boolean function using a K-map.

F(W,X,Y,Z) = ∑(0,1,2,3,5,6,8,9,10,12,13)

D = ∑(14), where D is a don’t care condition.

1. Design a sequential counter which counts from 0 to 5 and then starts again at 0. Implement with a T- flip flop or a D- flip flop. Specify the flip flop you will use. Illustrate the State Table, State Diagram and Sequential Circuit.
2. Implement the following functions:

F1 = AB’ + A’C+A’B’C’

F2 = ABC +A’BC’

Using:

1. A Programmable Logic Array(PLA)
2. A Programmable Array Logic (PAL) device
3. Explain the fundamental differences between the RAM and ROM memory modules.
4. Design a 3 to 8 decoder using basic elements: (AND, OR, INVERTER gates, etc).
5. Design a 4 to 1 multiplexer to implement the function: f(x,y,z)= ∑(0,1,2,4,5). You may use a block to represent the multiplexer, with the appropriate inputs, selection lines, and output.
6. Perform the following binary subtraction of unsigned numbers using two’s complement. Show your work. 100111 – 011111.