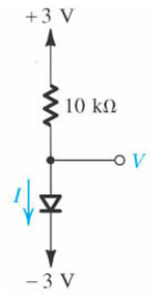
PRAIRIE VIEW A&M UNIVERSITY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
PhD PRELIMINARY EXAMS - MICROELECTRONICS
FALL 2016

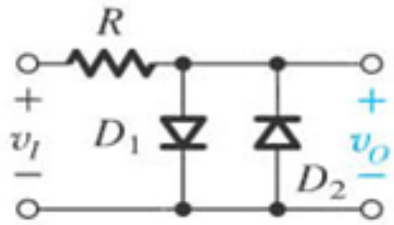
NAME: _____

Problem 1(a) (10 pts.) For circuit shown below, assuming that the voltage across a forward-biased conducting diode is 0.7 volts, Find the voltage V and I.



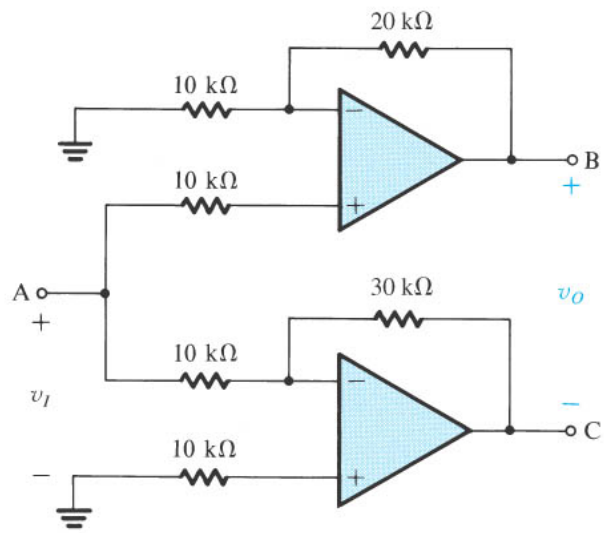
V = _____ I = _____

Problem 1(b) (6 points) Assuming that the voltage across a forward-biased conducting diode is 0.7 volts
find v_0 if V_I = -0.5V



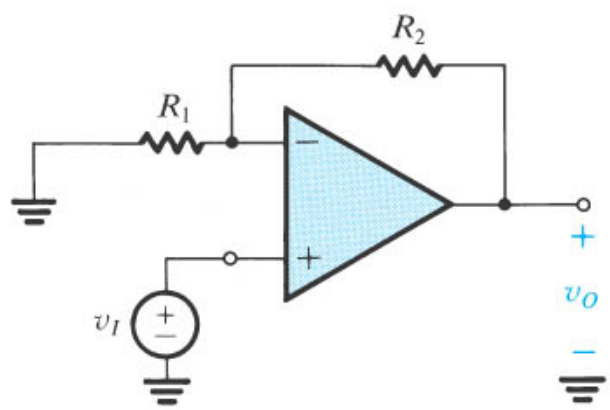
v_0 = _____

Problem 2(a) (12 points) If v_1 = 5 mV, (i) find the voltages at nodes B and C. (ii) Hence, calculate v_0.



Voltage at node B = _____ Voltage at node C = _____ v_0 = _____

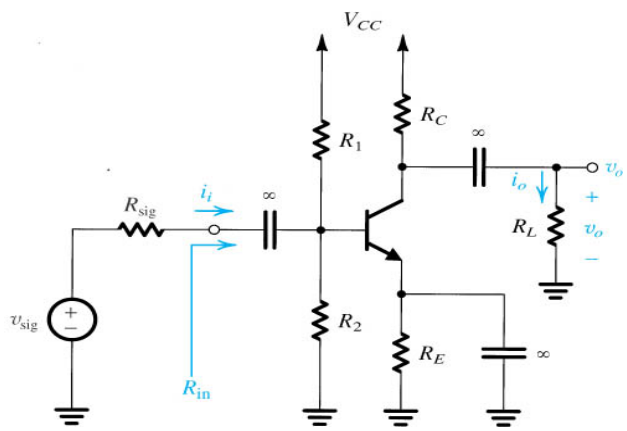
Problem 2(b) (6 points) For the amplifier shown below, what will be the range of the input voltage such that the output voltage of the op amp does not saturate at ± 15V. Assume that R_1 = 1 $K\Omega$, R_2 = 9 $K\Omega$,



Range of input voltage is from _____ to _____

Problem 3. (16 points) For the common-emitter amplifier shown below, V_{CC} is unknown, R_1 = 90 $K\Omega$, R_2 = 45 $K\Omega$, R_E = 1.0 $K\Omega$, R_C = 8.0 $K\Omega$, R_{sig} = 0.2 $K\Omega$, and R_L = 10 $K\Omega$. The transistor β is 100, r_O is almost infinite and r_π = 1.2 KΩ.

(a) Draw the small-signal equivalent circuit



Draw the small signal equivalent circuit here.

(b) Find the input resistance, R_{in},

(c) Determine voltage gain, $\frac{v_o}{v_{sig}}$.

Problem 4 (10 points)

A silicon p-n diode step junction maintained at room temperature is doped such that $E_F = E_v + E_G/5$ on the p-side and $E_F = Ec - k_BT$ on the n-side. Take the temperature as 300K and the bandgap as 1.1 eV

(a) Draw, to scale, the equilibrium energy band diagram for this junction.

(b) Determine, from the diagram, the built-in voltage V_{bi}.

Problem 5 (10 points)

In a p^+-n junction, suppose N_D is doubled. If everything else remains unchanged, which the of the following increase or decrease? Justify each answer.

PROPERTY	INCREASE/ DECREASE	JUSTIFICATION
Built-in Potential	Increases Decreases	
Junction Capacitance	Increases Decreases	
Breakdown Voltage	Increases Decreases	
Depletion Width	Increases Decreases	

Problem 6 (15 points)

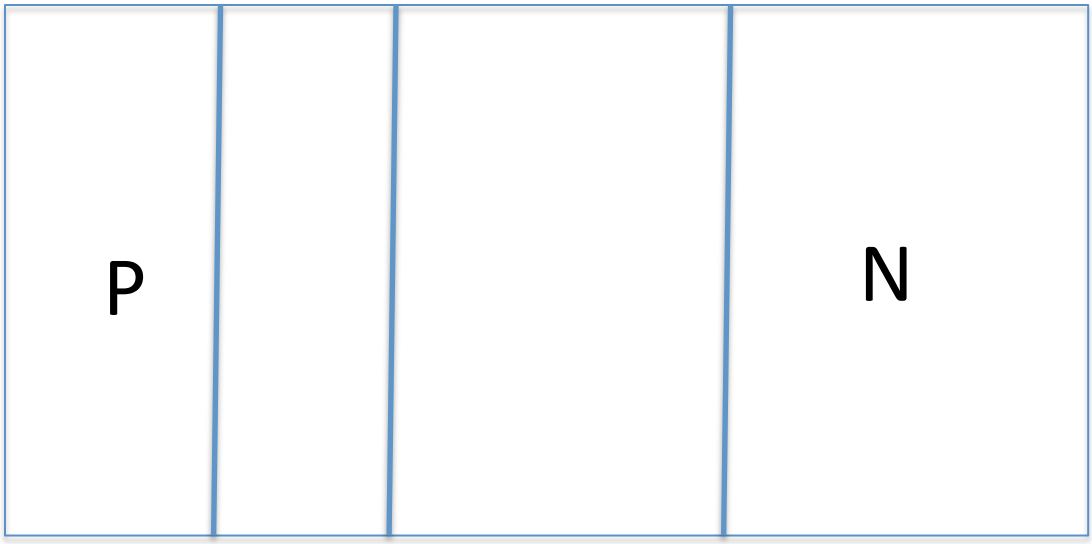
The current output of an optical diode is given by

$$I = I_0\left[1-\left(\frac{\phi}{\phi_0}\right)^2\right], \quad \phi_0 = \text{constant}$$

where ϕ is the voltage drop across the diode. Compute the maximum power output of this diode. [Hint: The power output is $I\phi$. The value $\phi = \phi_m$ at which the power is maximum is obtained by setting the first derivative is zero.]

Problem 7 (15 points)

The figure below is a schematic of p-n junction diode with the p-side and the n-side as shown. Label the various parts of the device appropriately by showing: the depletion region, space charge region, depletion widths on each side with the appropriate charges (donor and acceptor ions), majority and minority carriers (electrons and holes) on each side, the direction of electric field in the junction region, the directions of electron and hole diffusion, and the directions of electron and hole drift. Which side is more heavily doped?



Cheat Sheet - EE130

$q = 1.6*10^{-19}$ C $e_0 = 8.85*10^{-14}$ F/cm
K_S = 11.8, K_O = 3.9 Eg (Si) = 1.12 eV
Boltzman k = $8.62*10^{-5}$ eV/K
Planck h = $4.14*10^{-15}$ eV*s
Free e Mass, $m_0 = 9.1*10^{-31}$ kg
Effective density of states Nc = 3.22*10^19 cm-3
dEg = 3.5*10^(-8) * N^(1/3) eV

Basic Semiconductors Fundamentals

$f(E) = \frac{1}{1+e^{(E-E_f)/kT}}$ approx: $f(E) = e^{-(E-E_f)/kT}$

Charge Neutrality: $p-n+N_D-N_A=0$

$$n_i=\sqrt{N_C N_V e^{\frac{-E_G}{2kT}}} \qquad g_c(E)=\frac{m_n\sqrt{2m_n(E-E_C)}}{pi^2 h^3}$$

$$n=\frac{N_D-N_A}{2}+[(\frac{N_D-N_A}{2})^2+n_i^2]^{\frac{1}{2}}$$ Mn > Mp in Si

$$p=n_i e^{\frac{E_i-E_F}{kT}} \qquad E_i=\frac{E_c+E_v}{2}+\frac{3}{4}kTln(\frac{m_p}{m_n})$$

$$n=n_i e^{\frac{E_F-E_i}{kT}} \qquad E_F-E_i=kTln(\frac{n}{n_i})=-kTln(\frac{p}{n_i})$$

Low T = freeze out; high t = intrinsic; else extrinsic

$$J_P=J_{drift}+J_{diff}=q\mu_p pE-qD_P\frac{dp}{dx}$$

$$J_N=J_{drift}+J_{diff}=q\mu_n nE+qD_N\frac{dn}{dx}$$

mobility units cm^2/(s*V), diffusion = cm^2/s

Diff len.: $L_N=\sqrt{D_N\tau_n}$ $v_{th}=\sqrt{\frac{3kT}{m_{eff}}}$ $v=\mu E$

$$\frac{D}{\mu}=\frac{kT}{q} \qquad \mu_p=\frac{q\tau_{mp}}{m_p}, units: \frac{q\tau_{mp}}{m_p} \qquad F=\frac{-qE}{m_p}$$

hi T = phonon scattering, low T = ion scattering

$$\rho=\frac{1}{q(\mu_n n+\mu_p p)} \qquad \sigma=q(\mu_n n+\mu_p p)\Omega^{-1}cm^{-1}$$

Generation: band2band, R-G center, impact ion
Recomb: direct, R-G, Auger (2 collide, excite 1)

$$rate\ of\ recombination=\frac{dn}{dt}=\frac{\Delta n}{\tau}=\frac{\Delta p}{\tau}$$

Semiconductor Fabrication:

*oxidation = deposition of SiO2 layer
dry = thin, slow, precise, wet = thick, fast, imprecise
*lithography/etching = remove SiO2 with photoresist
*Dry/wet etch; dry=precise, wet = easy, cut sides
Antenna effect, charges left after etching, tunnel
*Ion Implantation = dopant atoms introduce into Si
low T vs diff. Dominant process now.
*Annealing/Diffusion = clean and spread
*Thin Film Deposition, spray metal, > clean sputter
*CVD – deposit ions/nitrides, etc.
Advanced lithography – EUV photo, ebeam, dip-pen
Positive = light, softens, negative = light hardens
Antenna effect – e- flow tunnel beneath oxide
Dop gasphase,solid source,in situ (deposit on surface)

PN Junctions

Forward Bias = Current flows P->N
Dep approx: assume carrier inside dep. region = 0
charge density out dep reg = 0 and q(Nd-Na) inside

$$\frac{d^2V}{dx^2}=\frac{-dE}{dx}=\frac{-\rho}{\epsilon_s} \quad \text{n:} \quad V(x)=V_{bi}-\frac{qN_D}{2\epsilon_s}(x_n-x)^2$$

$$W=\sqrt{\frac{2\epsilon_s(V_{bi}-V_A)}{q}(\frac{1}{N_A}+\frac{1}{N_D})}$$

$$v_{bi}=\frac{kT}{q}\ln(\frac{N_a N_d}{n_i^2}) \quad \text{p:} \quad V(x)=\frac{qN_A}{2\epsilon_s}(x+x_p)^2$$

n-side: $V(x)=V_{bi}-\frac{qN_D}{2\epsilon_s}(x_n-x)^2$

$N_A x_p=N_D x_n$ common field in depletion region
one that reaches first is first to depleted
Dep reg. Widens under reverse bias

E-field: $E(x)=\frac{-qN_A}{\epsilon_s}(x_p+x)$

Peak E-field: $E(0)=\frac{2qN}{\epsilon_s}(V_{bi}+|V_r|)^{1/2}$

Brkd Voltage: $V_{BR}=\frac{\epsilon_s E_{crit}^2}{2qN}-V_{bi}$

Cap diagram slope = $2/qN\epsilon_s A^2$

cap/volt characteristics: $\frac{1}{C_{dep}^2}=\frac{W_{dep}^2}{A^2\epsilon_s^2}=\frac{2(V_{bi}-V_A)}{qN\epsilon_s A^2}$

Vbr decreases with increasing N or decreasing Eg

$p_{p0}(-x_p)=N_A$ $n_{n0}(-x_n)=N_D$ majority

$n_{p0}(-x_p)=\frac{n_i^2}{N_A}$ $p_{n0}(-x_n)=\frac{n_i^2}{N_D}$ minority

$pn=n_i^2 e^{qV_A/kT}$ @ edge of dep region; maj/min

$n_p=n_{p0}+\Delta n_p(x)$ $p_n=p_{n0}+\Delta p_n(x)$

Drift doesn't change with V b/c low numbers
Forward bias = more minority @ dep edge
Reverse bias = black hole @ dep edge

$$\frac{\partial\Delta n_p}{\partial t}=D_N\frac{\partial^2\Delta n_p}{\partial x^2}-\frac{\Delta n_p}{\tau_n}+G_L \quad \text{assume E = 0}$$

$$\frac{\partial\Delta p_n}{\partial t}=D_P\frac{\partial^2\Delta p_n}{\partial x^2}-\frac{\Delta p_n}{\tau_p}+G_L \qquad L_p=\sqrt{D_p\tau_p}$$

Steady State: $\frac{\partial\Delta p_n}{\partial t}\to 0$

No gradient/diff current: $D_P\frac{\partial^2\Delta p_n}{\partial x^2}\to 0$

No thermal R-G: $\frac{\Delta p_n}{\tau_p}\to 0$ No light: $G_L\to 0$

Diode Saturation Currents:

$$I_0=Aqn_i^2(\frac{D_p}{L_p N_d}+\frac{D_n}{L_n N_a}) \qquad I=I_0(e^{qV/kT}-1)$$

IV curve shifts left @ high T b/c more diffusion
Charge storage: $I=Q/\tau_s$ charge/carrier lifetime

Capacitance: $C=\tau_s G$ Conductance: $G=\frac{I_{DC}q}{kT}$

PIN Junctions

Only e/h generated in dep reg contribute to current
Only light absorbed in dep reg is useful. Avalanches.

MS Junctions

lightly doped rectifying, heavily doped ohmic
Ideal assumptions: intimate contact, no oxide/charge
Not ideal: interface pinned Ef 0.4-0.9 eV below Ec

$\Phi_{BN}=\Phi_M-X$ Barrier height; work(metal) – EA

$\Phi_{BN}=qV_{bi}+[\frac{1}{2}E_G-(E_{FS}-E_i)_{FB}]$ barrier height

$\Phi_{BP}=X+E_G-\Phi_M$ holes' barrier

$V_{bi}=\Phi_M-\Phi_S=\Phi_B-(E_C-E_F)$ built-in potential

$$W=\sqrt{\frac{2\epsilon_s(V_{bi}-V_A)}{qN_D}}=\sqrt{\frac{2\epsilon_s(V_{bi}+V_A)}{qN_A}}$$