Chapter 7

Hardware Details of the 68000

Objectives
- The general specifications of the 68000 microprocessor
- The processor’s control signal names and functions
- General signal relationships and timing
- Methods in which the 68000 may interface with external devices
- The external interrupt signals and their operations
- The 68000's bus arbitration scheme
- The method used to access a peripheral
- How hardware expansion is provided by a bus connector

Introduction
- Before using any microprocessor, we must know both its hardware requirements and its software functions
- After this chapter, we should know about the various signals of the 68000

CPU Specifications
- 68000 is a 16-bit microprocessor with a 16-bit bi-directional data bus
- 24-bit address bus can address up to 16MB
- 3 interrupt lines provide 7 levels of external interrupts
- 3 control outputs may decode eight internal CPU states
- Clock speeds from 4 to 16MHz

CPU Pin Descriptions

Vcc, GND, and CLK
- 2 pins each for Vcc and 2 GND
- Single supply voltage of 4.75—5.25V
- Dissipate 1.5W of power with 8MHz, how about the required supply current?
- CLK: TTL-compatible waveform and 10ns for rise and fall times
Vcc, GND, and CLK

+5 V

Clock circuit

Crystal

FCC, VCC

CLK 68000

GND GND

FC0, FC1, and FC2

- Function code outputs, they indicate the current internal processing state of the 68000
- They are only valid when the AS signal is active
- Can use 74LS138 to decode

FC0, FC1, and FC2

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<th>FC0</th>
<th>Cycle type</th>
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*By Motorola, for future use.

Interrupt Acknowledge Decoder

E, VMA, and VPA

- Give 68000 capability to control older 68000 peripherals
- E - E clock
- VMA - valid memory address
- VPA - valid peripheral address
- Only VPA is an input
6800 Peripheral Timing and Interface

RESET, HALT, and BERR
- For system control
- BERR – bus error

IPL0, IPL1, and IPL2
- For interrupt control
- 7 levels of interrupt

Br, BG, and BGACK
- For bus arbitration control
- BR – bus request
- BG – bus grant
- BGACK – bus grant acknowledge
- Why BGACK?
**BR, BG, and BGACK**

- Address bus
- Data bus
- Control bus

**AS, R/W, UDS, LDS, and DTACK**

- Asynchronous bus control
- AS – address strobe
- R/W – read/write
- UDS, LDS – upper/lower data strobe
- DTACK – data transfer acknowledge

**Decoding Memory Read/Write Signals**

- A1 Through A23
- D0 Through D15

**Address and data bus**

**Signal Summary**

**System Timing Diagrams – Processor HALT Timing**
System Timing Diagrams – Bus Arbitration Timing

Providing Access to the Processor Signals
- Expansion connector allows users to add functionality to the computer system
- Macintosh SE personal computer – 96-pin SE Bus
- Macintosh II – 96-pin NuBus

Troubleshooting Techniques and Summary
- To be familiar with all the 68000’s signals
- All 68000’s signals are covered in this chapter
- We also looked at two timing examples